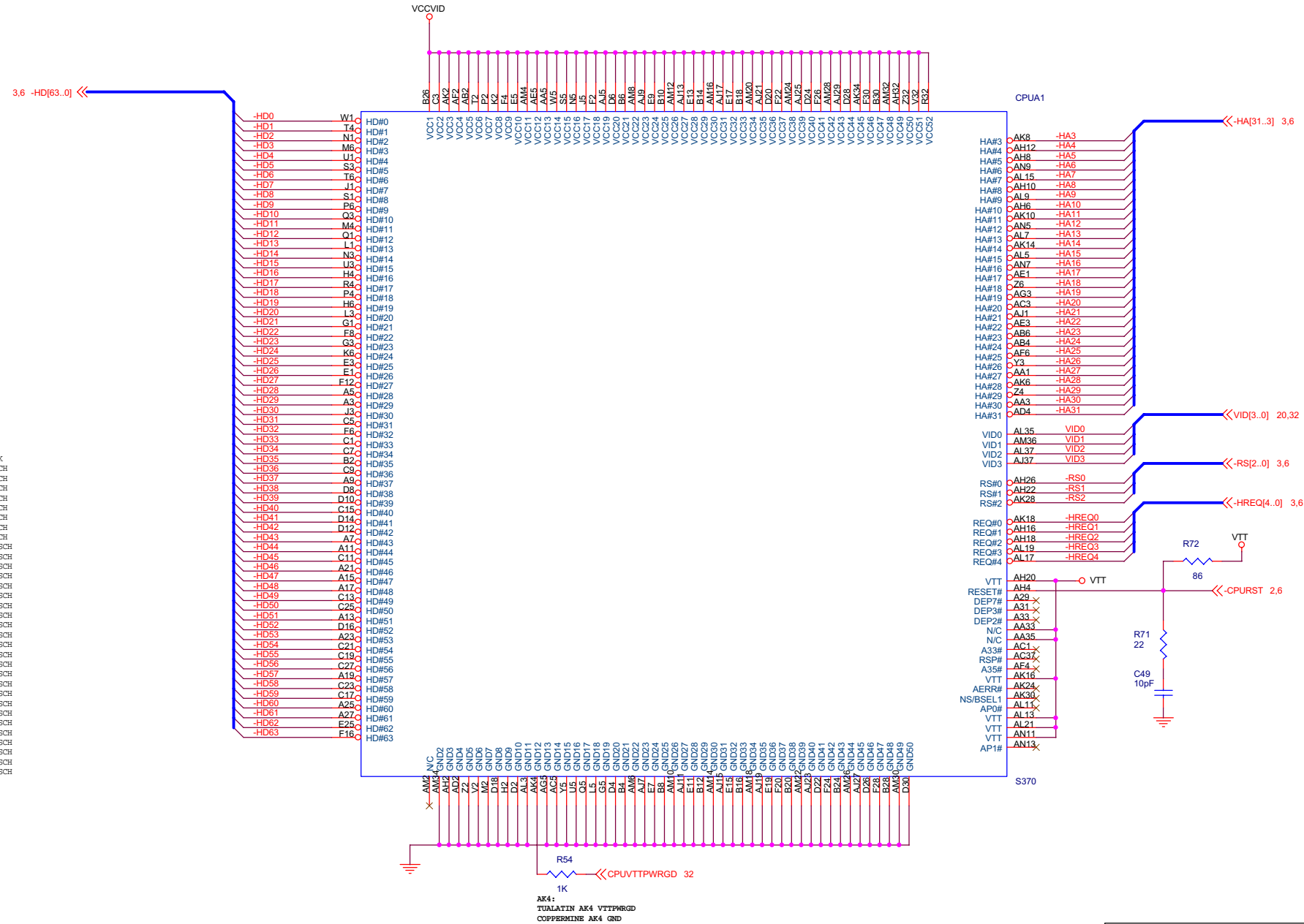
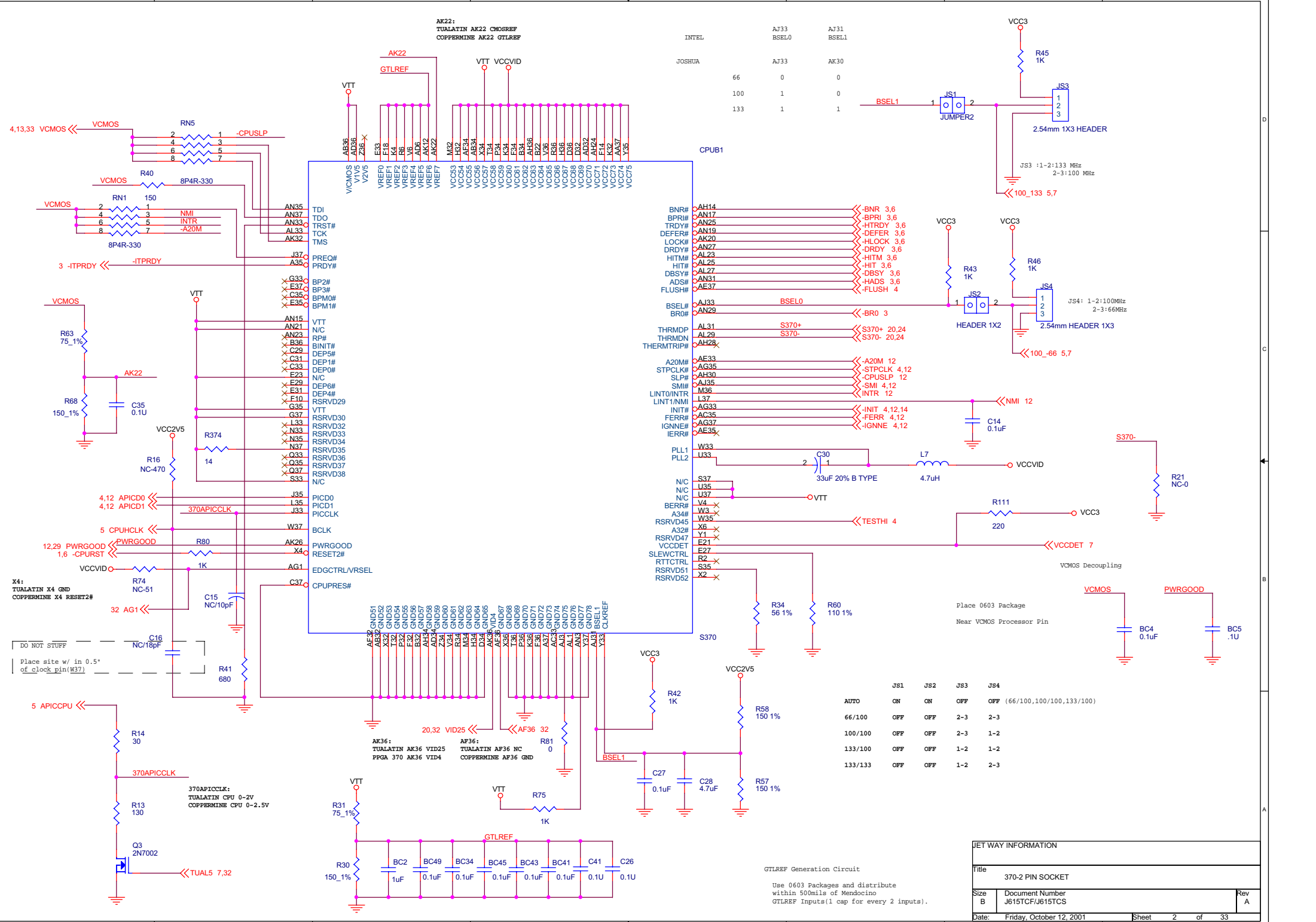
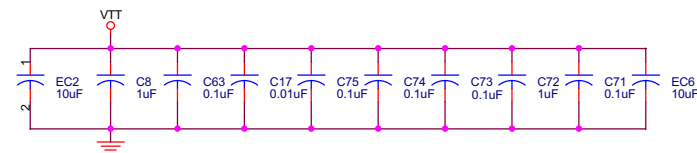
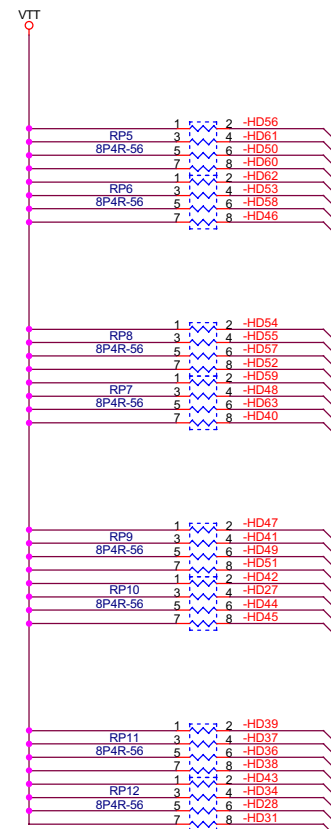
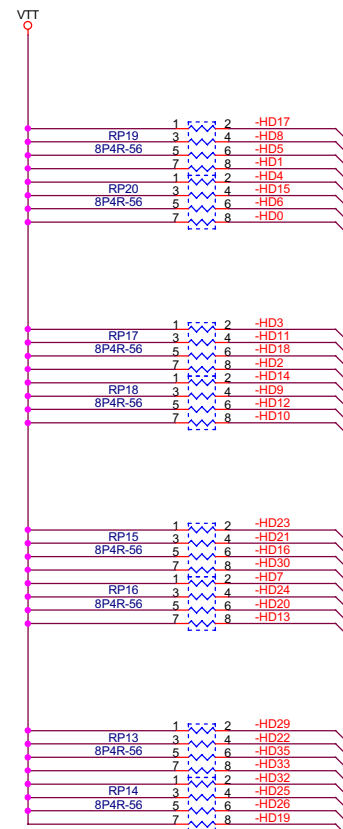
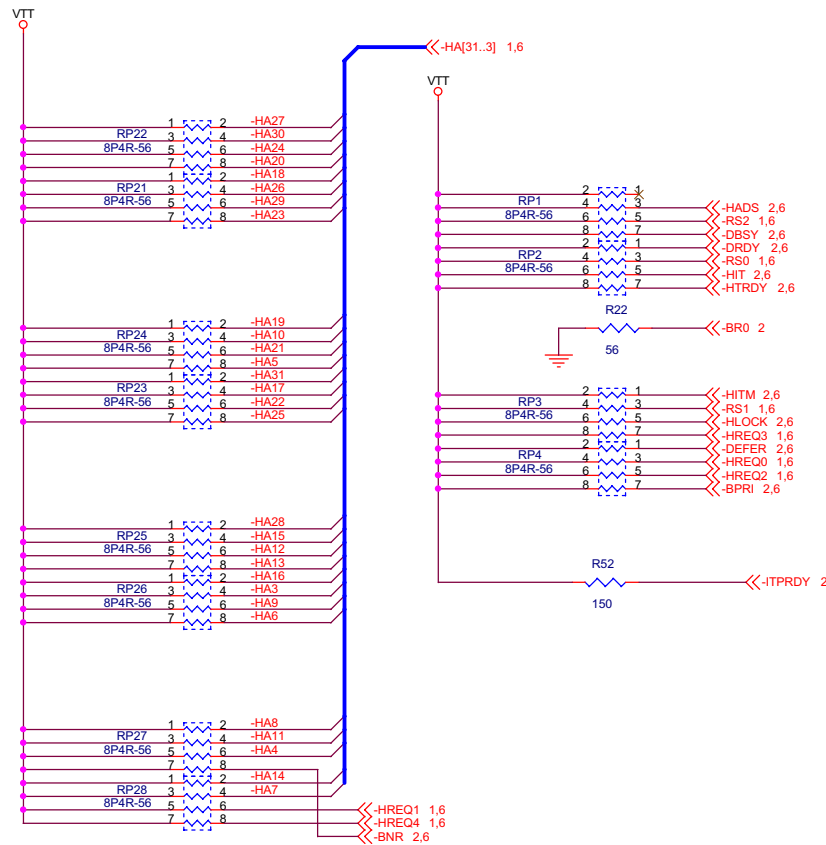


- 1. LNK
- 2. SCH
- 3. SCH
- 4. SCH
- 5. SCH
- 6. SCH
- 7. SCH
- 8. SCH
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- 32. SCH
- 33. SCH

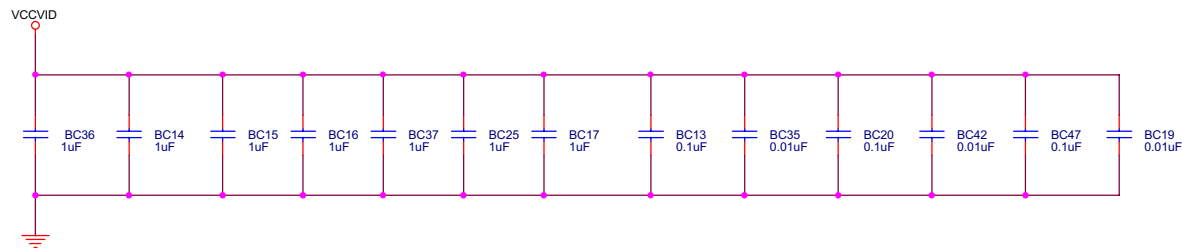


JET WAY INFORMATION		
Title	370-1 PIN SOCKET	
Size	Document Number	Rev
B	J615TCF/J615TCS	A
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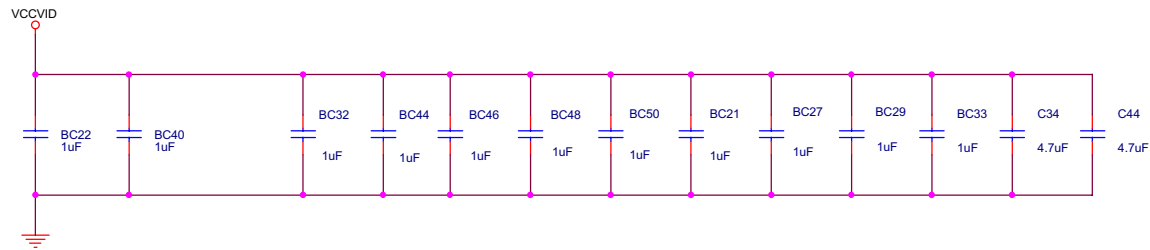




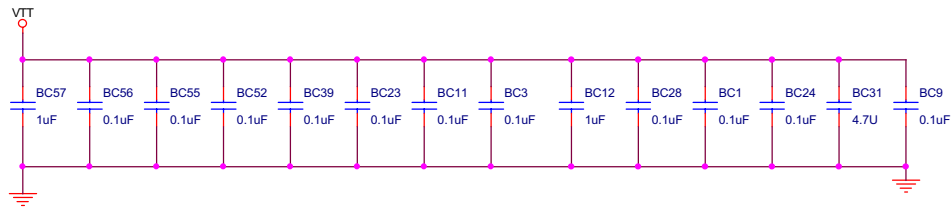
JET WAY INFORMATION		
Title	GTL Termination	
Size	Document Number	Rev
B	J615TCF/J615TCS	A
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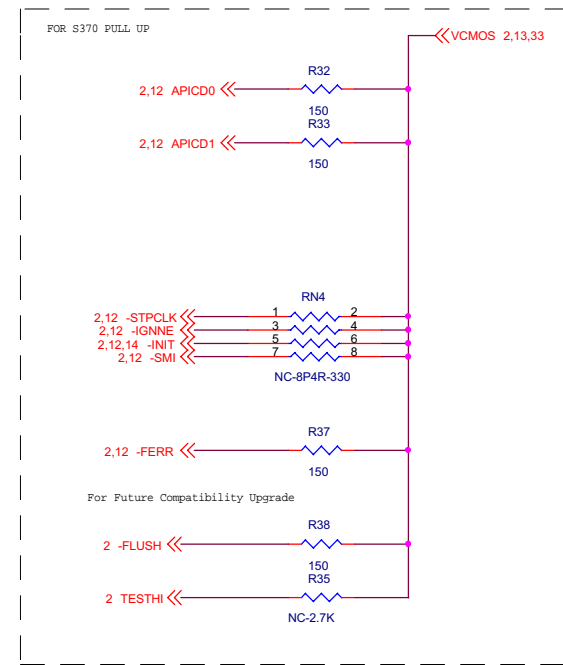
FOR CPU



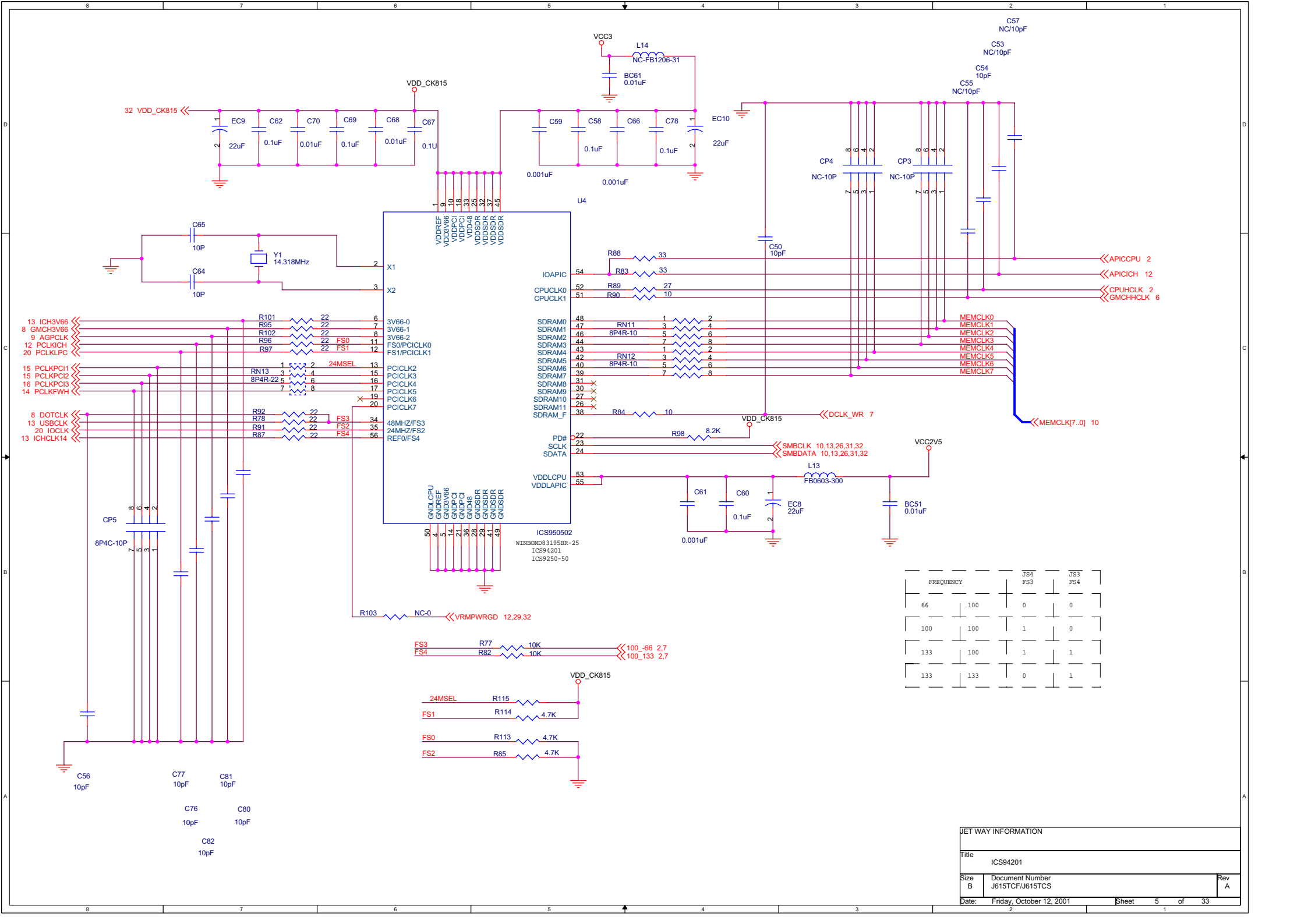
FOR CPU



FOR CPU VTT



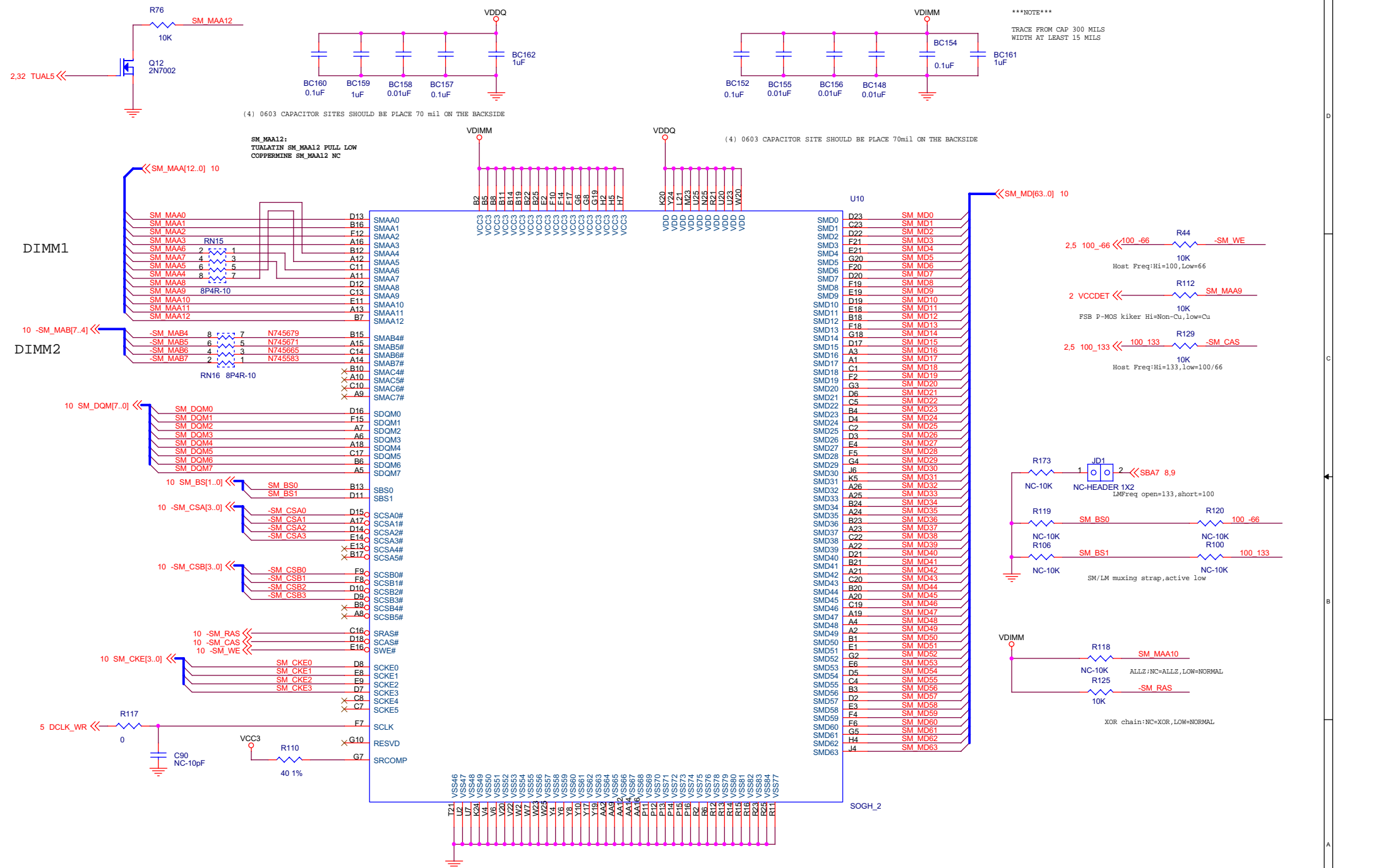
JET WAY INFORMATION		
Title	370-pin Socket Decoupling	
Size	Document Number	Rev
B	J615TCF/J615TCS	A
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FREQUENCY	J54 FS3	J53 FS4
66	100	0
100	100	1
133	100	1
133	133	0

JET WAY INFORMATION		
Title	ICS94201	
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B	J615TCF/J615TCS	A
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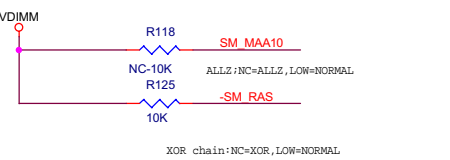
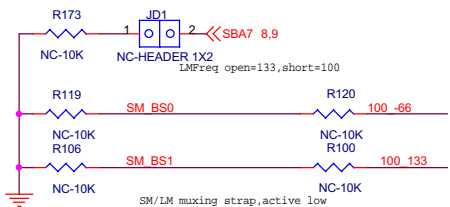


\*\*\*NOTE\*\*\*  
TRACE FROM CAP 300 MILS  
WIDTH AT LEAST 15 MILS

(4) 0603 CAPACITOR SITES SHOULD BE PLACE 70 mil ON THE BACKSIDE

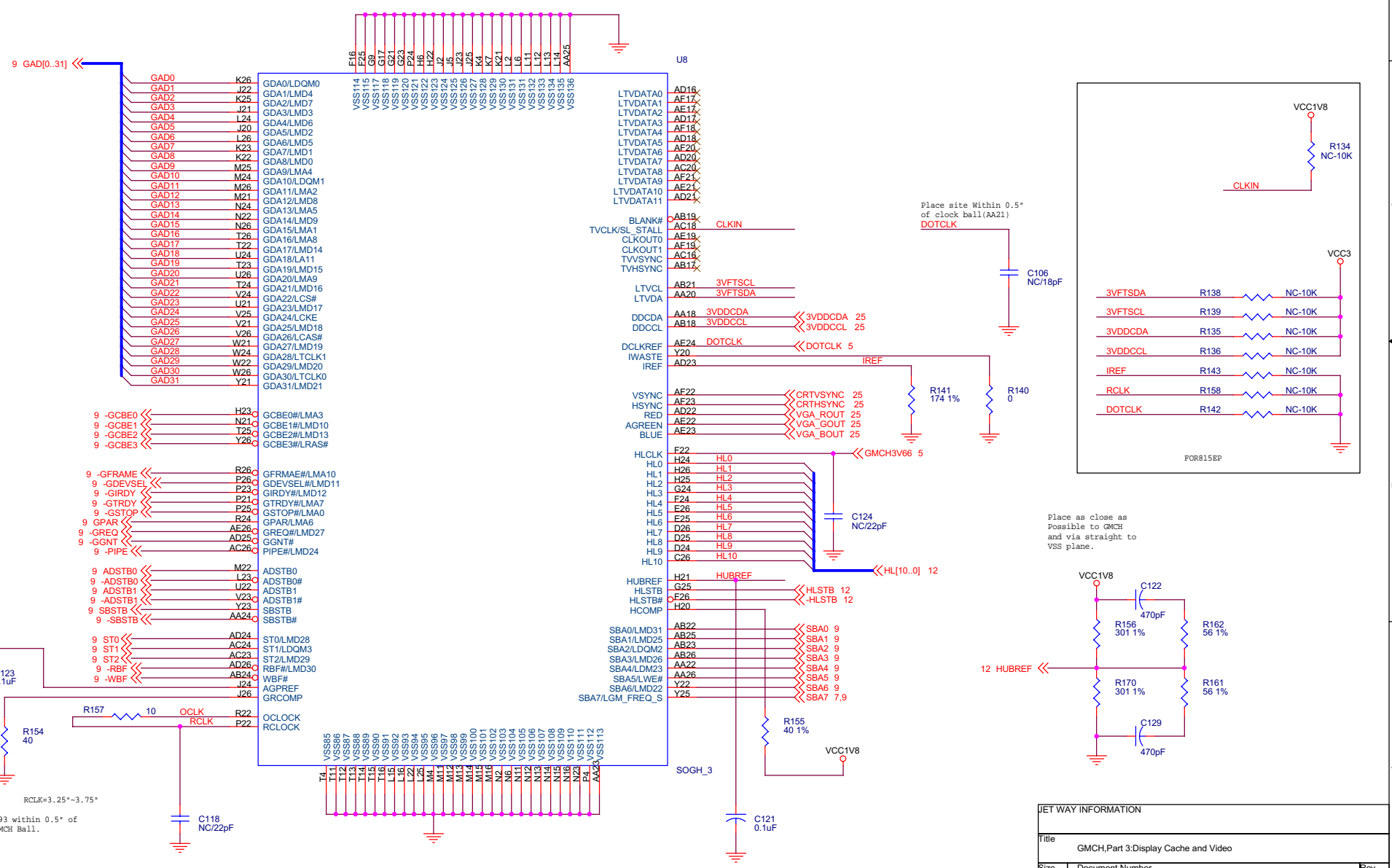
(4) 0603 CAPACITOR SITE SHOULD BE PLACE 70mil ON THE BACKSIDE

SM\_MAA12:  
TUALATIN SM\_MAA12 PULL LOW  
COPPERMINE SM\_MAA12 NC



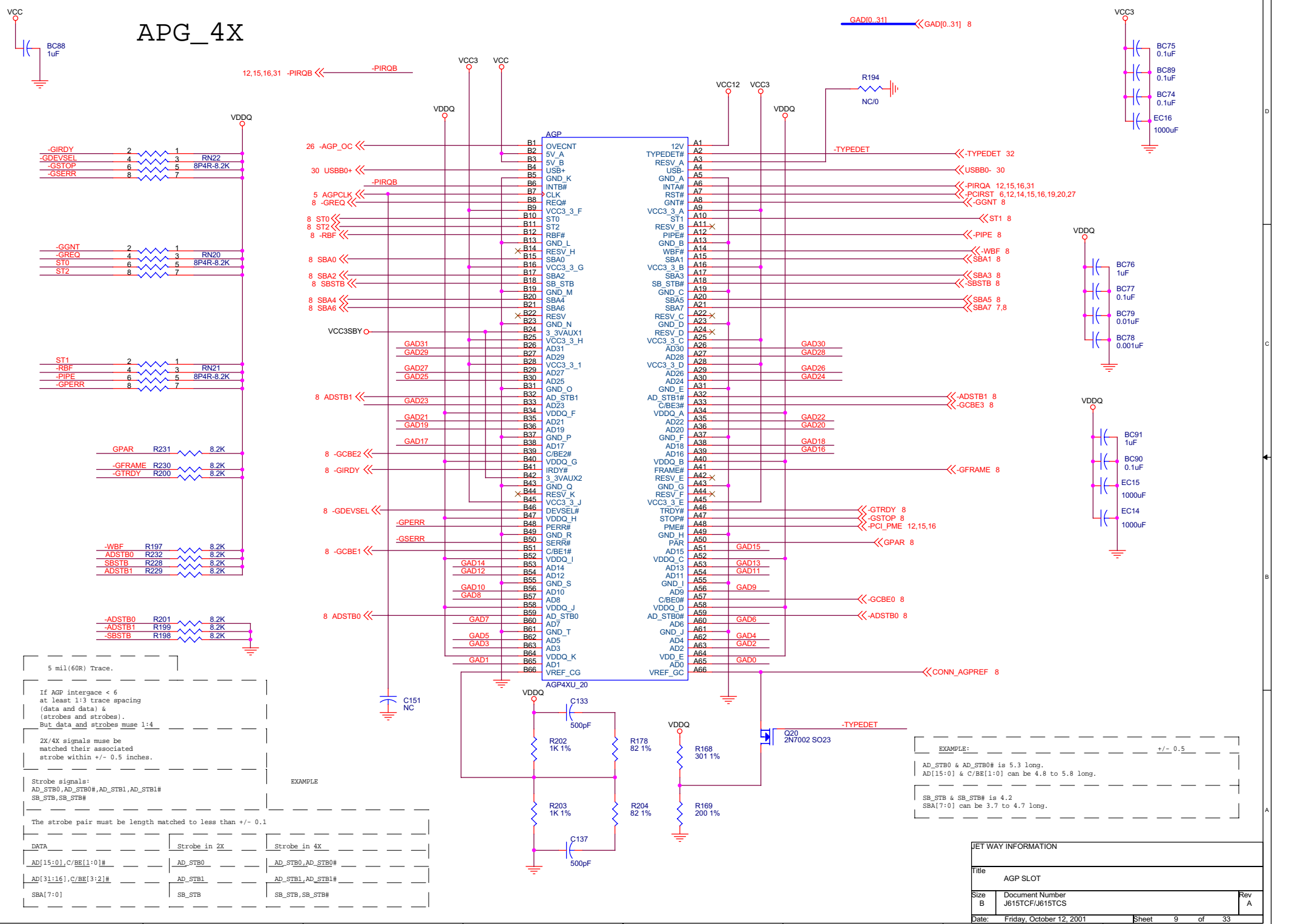
JET WAY INFORMATION		
Title GMCH,Part2:System Memory and Hub		
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Use surface mount caps placed close as possible to power pins with short, wide direct connections.



JET WAY INFORMATION		
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# APG\_4X



5 mil (60R) Trace.

If AGP intergrace < 6 at least 1:3 trace spacing (data and data) & (strokes and strokes). But data and strokes muse 1:4

2X/4X signals muse be matched their associated strobe within +/- 0.5 inches.

Strobe signals:  
AD\_STB0, AD\_STB0#, AD\_STB1, AD\_STB1#  
SB\_STB, SB\_STB#

The strobe pair must be length matched to less than +/- 0.1

DATA	Strobe in 2X	Strobe in 4X
AD[15:0], C/BE[1:0]#	AD_STB0	AD_STB0, AD_STB0#
AD[31:16], C/BE[3:2]#	AD_STB1	AD_STB1, AD_STB1#
SBA[7:0]	SB_STB	SB_STB, SB_STB#

EXAMPLE

EXAMPLE:

AD\_STB0 & AD\_STB0# is 5.3 long.  
AD[15:0] & C/BE[1:0] can be 4.8 to 5.8 long.

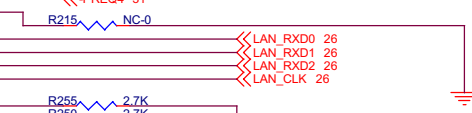
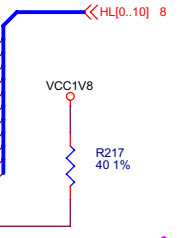
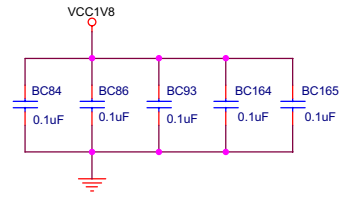
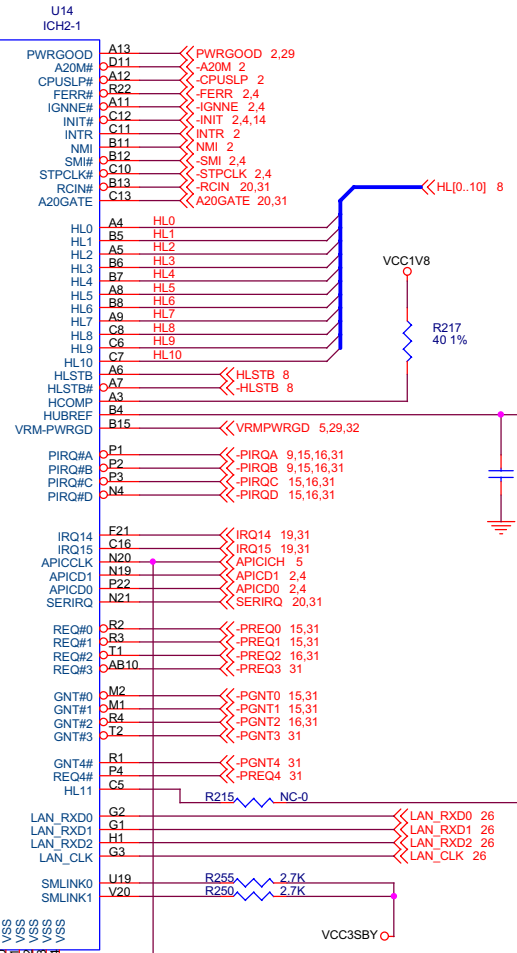
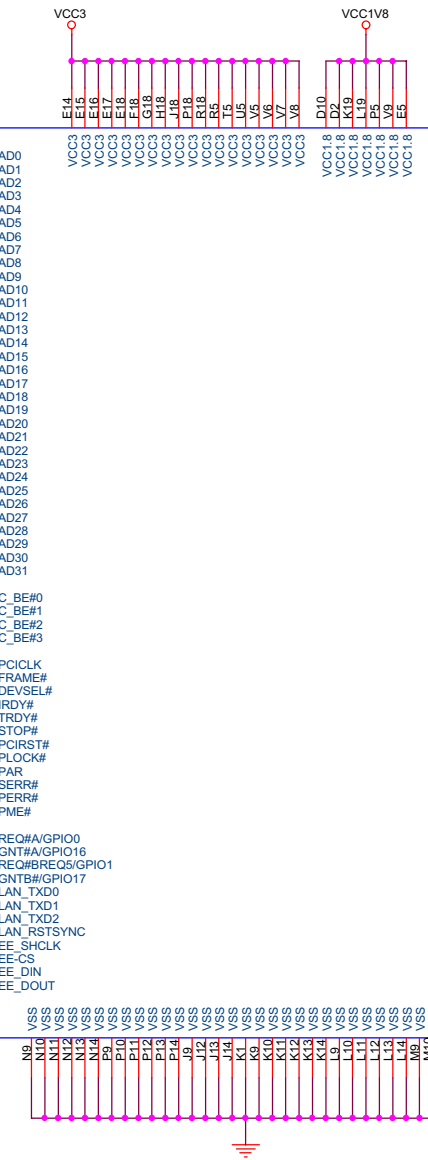
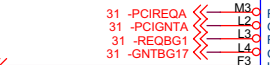
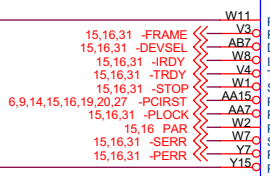
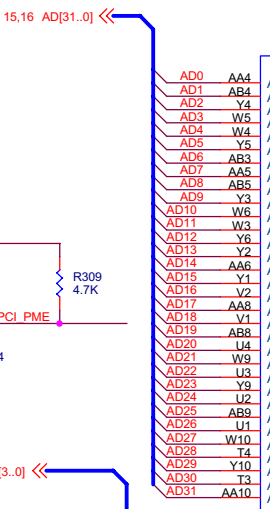
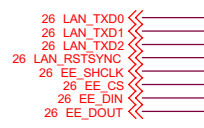
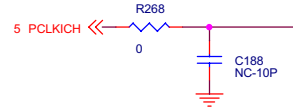
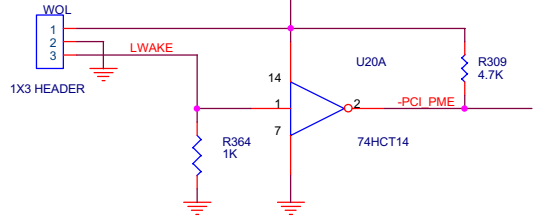
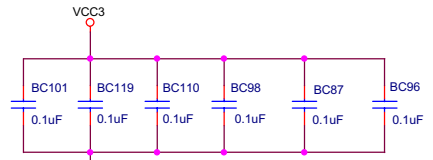
SB\_STB & SB\_STB# is 4.2  
SBA[7:0] can be 3.7 to 4.7 long.

JET WAY INFORMATION		
Title	AGP SLOT	
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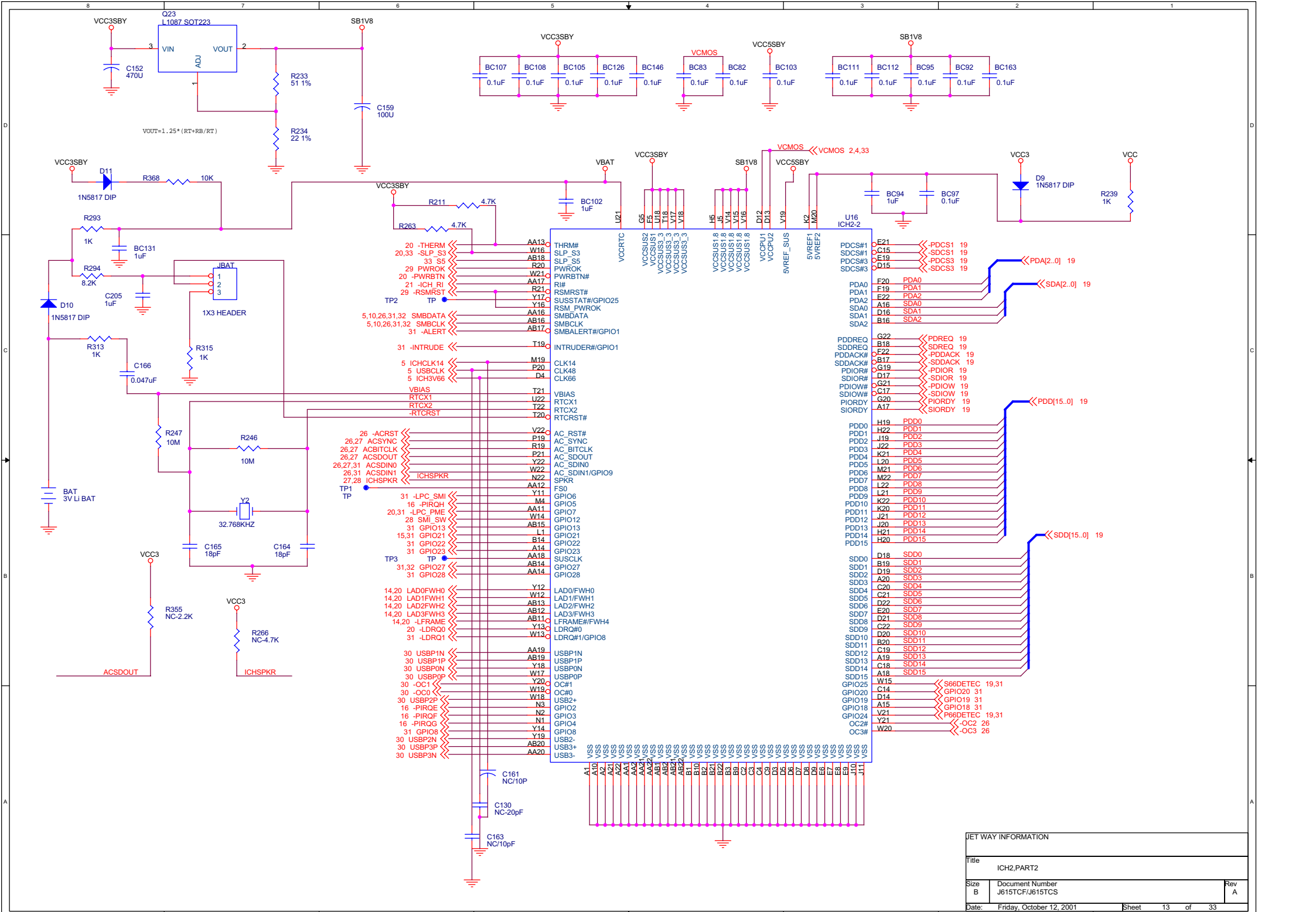


RESERVED

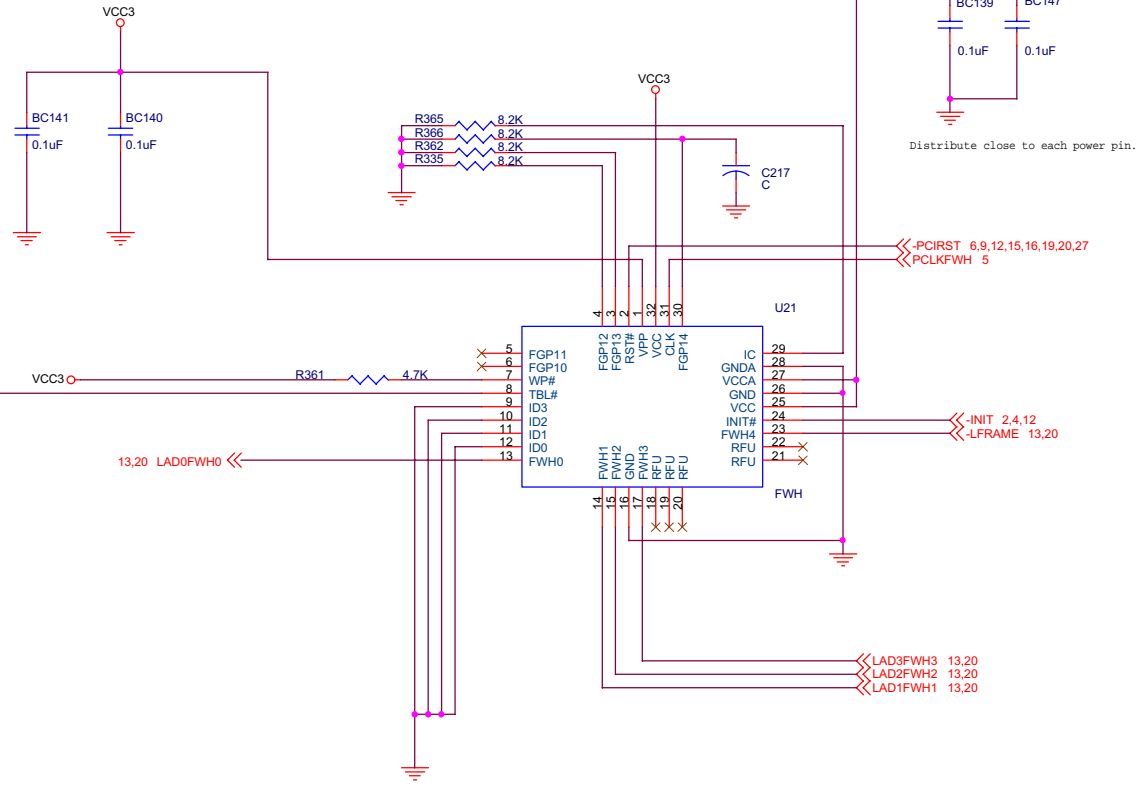
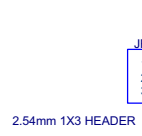
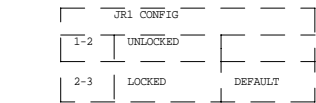
JET WAY INFORMATION			
Title		RESERVED	
Size	Document Number	Rev	
B	J615TCF/J615TCS	A	
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JET WAY INFORMATION			
Title ICH2,PART1			
Size B	Document Number J615TCF/J615TCS	Rev A	
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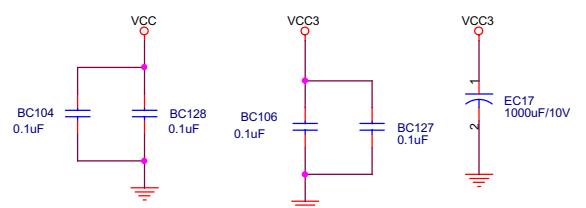
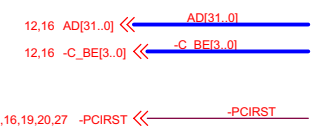
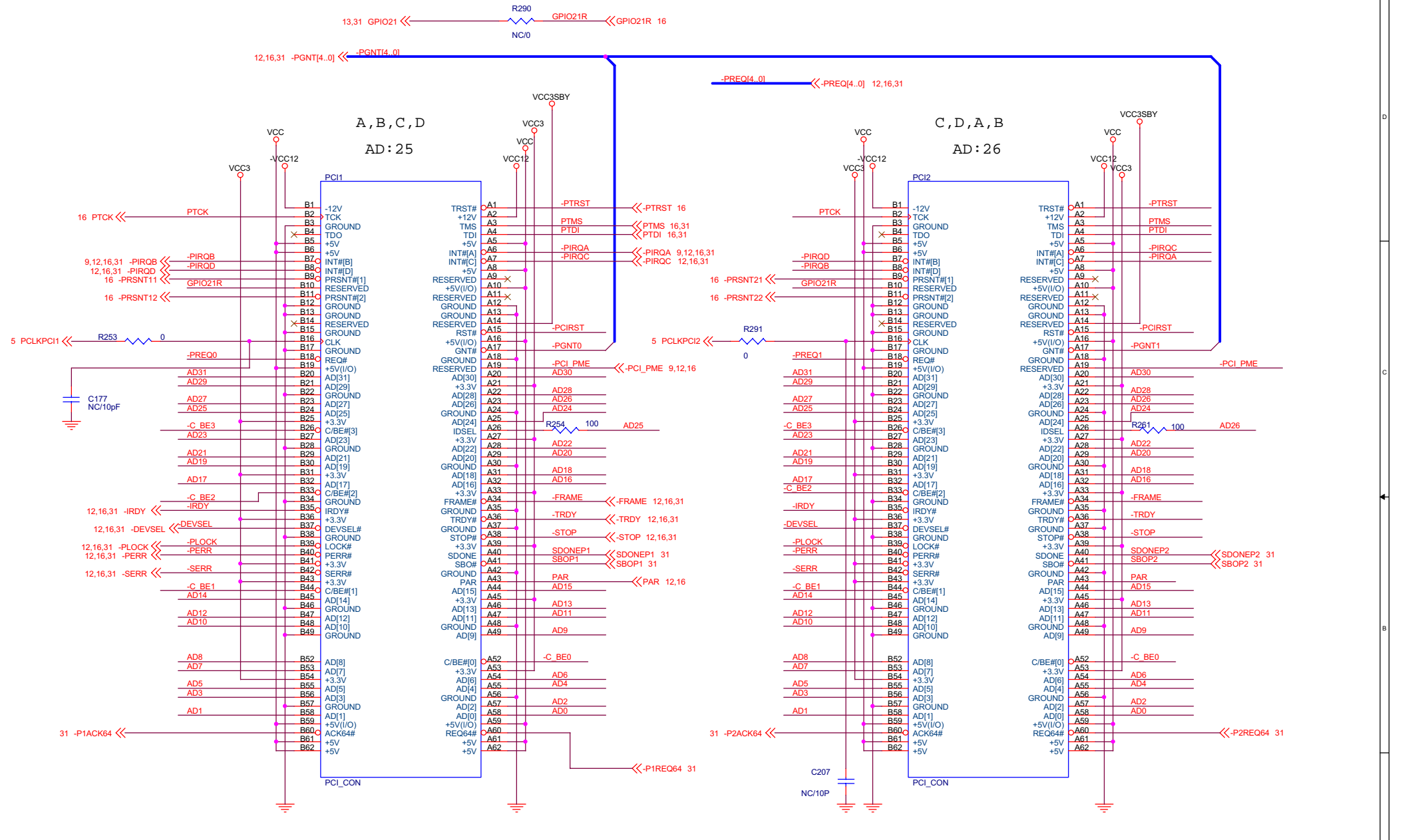
20 -THERM	THRM#	AA13	THRM#	AA13
20,33 -SLP_S3	SLP_S3	W16	SLP_S3	W16
33 -S3	SLP_S5	AB18	SLP_S5	AB18
29 -PWROK	PWR#OK	R20	PWR#OK	R20
20 -PWRBTN	PWRBTN#	W21	PWRBTN#	W21
21 -ICH_RI	RI#	AA17	RI#	AA17
29 -RSMRST	RSMRST#	R21	RSMRST#	R21
TP2	SUSSTAT#/GPIO25	Y17	SUSSTAT#/GPIO25	Y17
TP	RSM_PWROK	Y12	RSM_PWROK	Y12
5,10,26,31,32 -SMBDATA	SMBDATA	Y16	SMBDATA	Y16
5,10,26,31,32 -SMBCLK	SMBCLK	AA16	SMBCLK	AA16
31 -ALERT	SMBALERT#/GPIO1	AB16	SMBALERT#/GPIO1	AB16
31 -INTRUDE	INTRUDER#/GPIO1	AB17	INTRUDER#/GPIO1	AB17
TP1	T19	T19	T19	T19
5 ICHCLK14	CLK14	M19	CLK14	M19
5 USBCLK	CLK48	P20	CLK48	P20
5 ICH3V66	CLK66	D4	CLK66	D4
VBIA	VBIA	T21	VBIA	T21
RTCX1	RTCX1	U22	RTCX1	U22
RTCX2	RTCX2	T22	RTCX2	T22
-RTCRST	RTCRST#	T20	RTCRST#	T20
26 -ACRST	AC_RST#	V22	AC_RST#	V22
26,27 ACSYNC	AC_SYNC	P19	AC_SYNC	P19
26,27 ACBITCLK	AC_BITCLK	R19	AC_BITCLK	R19
26,27 ACSDOOUT	AC_SDOOUT	P21	AC_SDOOUT	P21
26,27,31 ACSDINO	AC_SDOIN0	Y22	AC_SDOIN0	Y22
26,31 ACSDIN1	AC_SGIN1/GPIO9	W22	AC_SGIN1/GPIO9	W22
27,28 ICHSPKR	SPKR	N22	SPKR	N22
TP3	FS0	AA12	FS0	AA12
31 -LPC_SMI	GPIO6	Y11	GPIO6	Y11
16 -PIRQH	GPIO5	M4	GPIO5	M4
20,31 -LPC_PME	GPIO7	AA11	GPIO7	AA11
28 SMI_SW	GPIO12	W14	GPIO12	W14
31 GPIO13	GPIO13	AB15	GPIO13	AB15
15,31 GPIO21	GPIO21	L1	GPIO21	L1
31 GPIO22	GPIO22	B14	GPIO22	B14
31 GPIO23	GPIO23	A14	GPIO23	A14
31 GPIO28	GPIO28	AA18	GPIO28	AA18
TP	SUSCLK	AB14	SUSCLK	AB14
31,32 GPIO27	GPIO27	AA14	GPIO27	AA14
31 GPIO28	GPIO28	AA14	GPIO28	AA14
14,20 LAD0FWH0	LAD0/FWH0	Y12	LAD0/FWH0	Y12
14,20 LAD1FWH1	LAD1/FWH1	W12	LAD1/FWH1	W12
14,20 LAD2FWH2	LAD2/FWH2	AB13	LAD2/FWH2	AB13
14,20 LAD3FWH3	LAD3/FWH3	AB12	LAD3/FWH3	AB12
14,20 -LFRAME	LFRAME#/FWH4	AB11	LFRAME#/FWH4	AB11
20 -LDRQ0	LDRQ#0	Y13	LDRQ#0	Y13
31 -LDRQ1	LDRQ#1/GPIO8	W13	LDRQ#1/GPIO8	W13
30 USBP1N	USBP1N	AA19	USBP1N	AA19
30 USBP1P	USBP1P	AB19	USBP1P	AB19
30 USBP0N	USBP0N	Y18	USBP0N	Y18
30 USBP0P	USBP0P	W17	USBP0P	W17
30 -OC1	OC#1	Y20	OC#1	Y20
30 -OC0	OC#0	W19	OC#0	W19
30 USBP2P	USB2+	N3	USB2+	N3
16 -PIRQ	GPIO2	N2	GPIO2	N2
16 -PIRQF	GPIO3	N1	GPIO3	N1
16 -PIRQG	GPIO4	N1	GPIO4	N1
31 GPIO8	GPIO8	Y14	GPIO8	Y14
30 USBP2N	USB2-	Y19	USB2-	Y19
30 USBP3P	USB3+	AB20	USB3+	AB20
30 USBP3N	USB3-	AA20	USB3-	AA20
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VSS	VSS	A0	VSS	A0
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VSS	VSS	AA154	VSS	AA154
VSS	VSS	AA155	VSS	AA155
VSS	VSS	AA156	VSS	AA156
VSS	VSS	AA157	VSS	AA157
VSS	VSS	AA158	VSS	AA158
VSS	VSS	AA159	VSS	AA159
VSS	VSS	AA160	VSS	AA160
VSS	VSS	AA161	VSS	AA161
VSS	VSS	AA162	VSS	AA162
VSS	VSS	AA163	VSS	AA163
VSS	VSS	AA164	VSS	AA164
VSS	VSS	AA165	VSS	AA165
VSS	VSS	AA166	VSS	AA166
VSS	VSS	AA167	VSS	AA167
VSS	VSS	AA168	VSS	AA168
VSS	VSS	AA169	VSS	AA169
VSS	VSS	AA170	VSS	AA170
VSS	VSS	AA171	VSS	AA171
VSS	VSS	AA172	VSS	AA172
VSS	VSS	AA173	VSS	AA173
VSS	VSS	AA174	VSS	AA174
VSS	VSS	AA175	VSS	AA175</



NOTES:

VPP and WP# are tied to VCC3 in this configuration Write Protection is register based with the exception of the Boot Block.

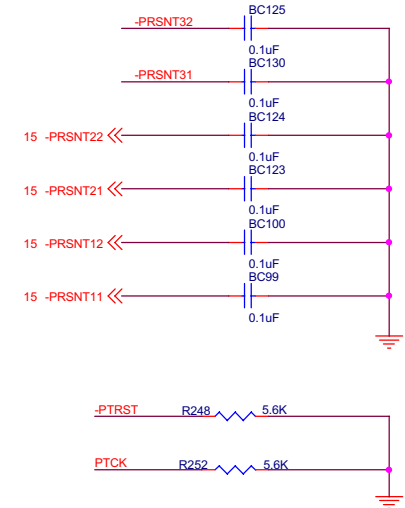
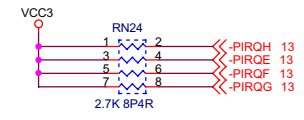
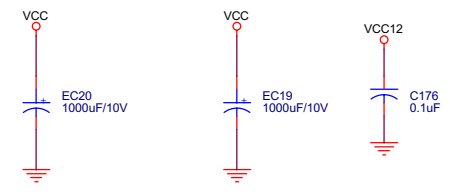
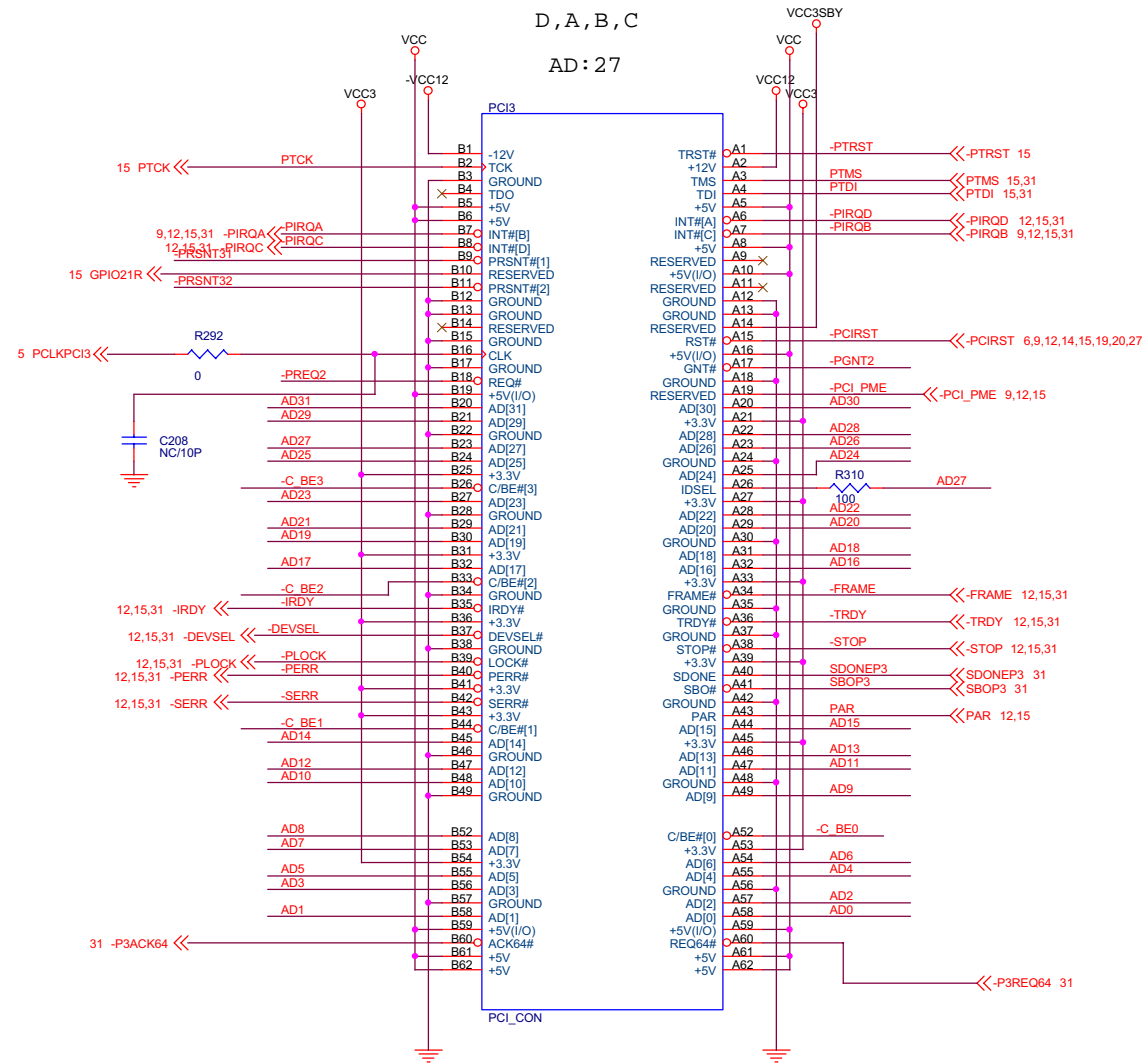
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Size	Document Number	Rev
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JET WAY INFORMATION		
Title PCI CONNECTOR 1 & 2		
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-PGNT[4..0] <<-PGNT[4..0] 12,15,31  
 -PREQ[4..0] <<-PREQ[4..0] 12,15,31

D, A, B, C  
 AD: 27



12,15 -C\_BE[3..0] <<-C\_BE[3..0]  
 12,15 AD[31..0] <<AD[31..0]

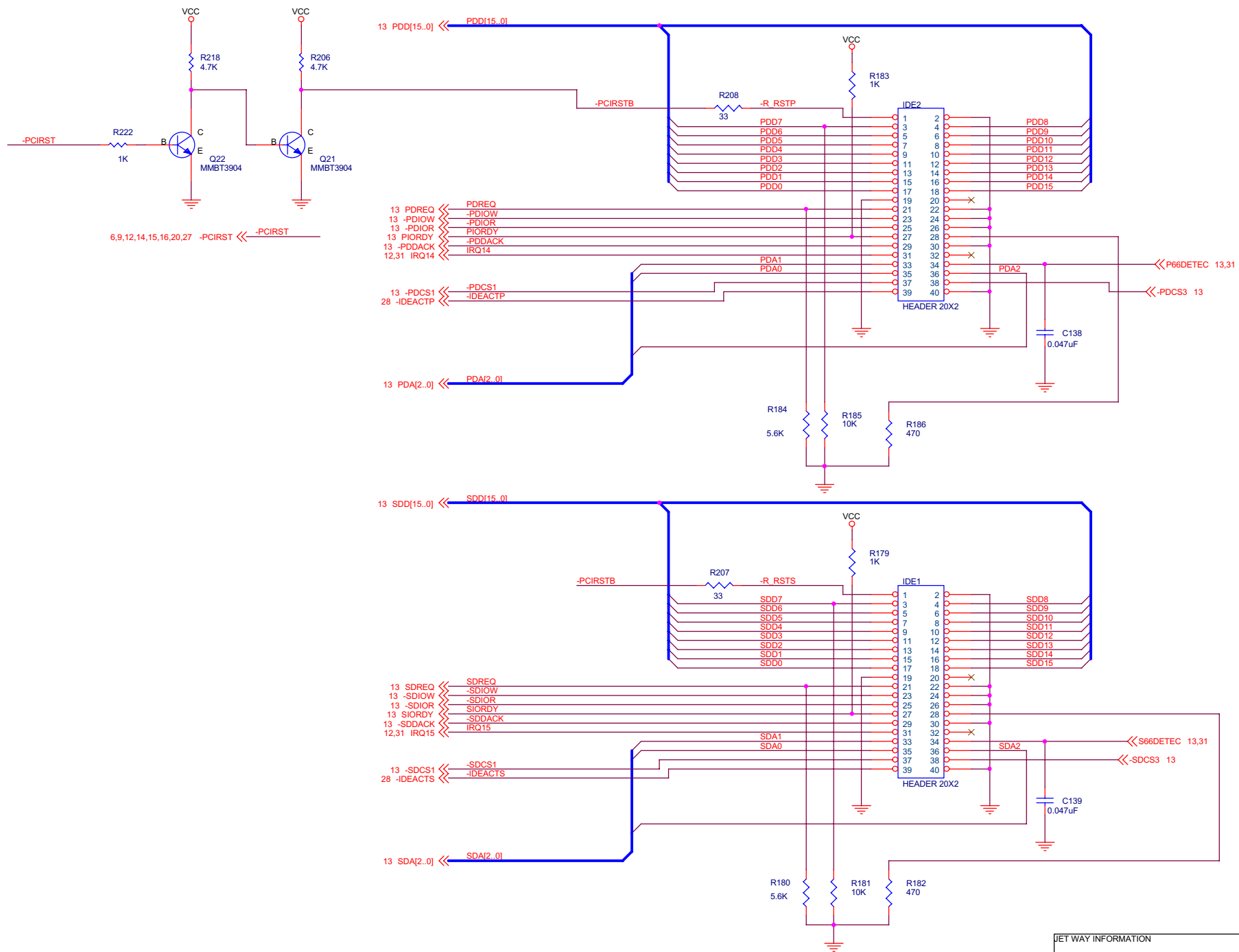
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Size B	Document Number J615TCF/J615TCS	Rev A
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RESERVED

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Size	Document Number	Rev	
B	J615TCF/J615TCS	1	
Date:	Friday, October 12, 2001	Sheet	17 of 33

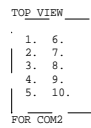
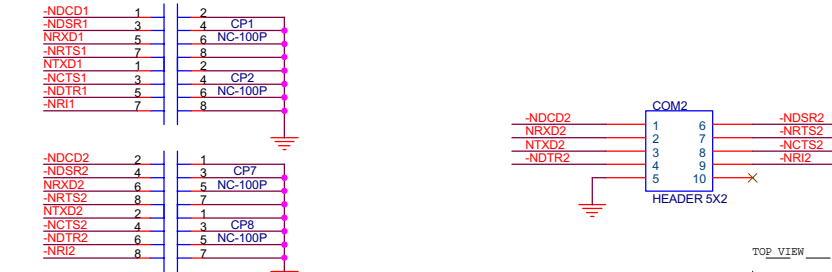
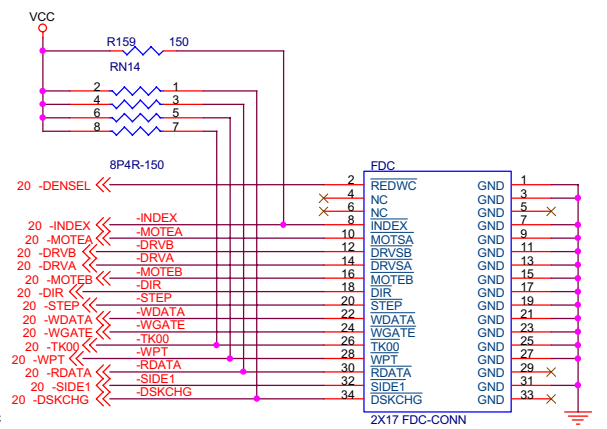
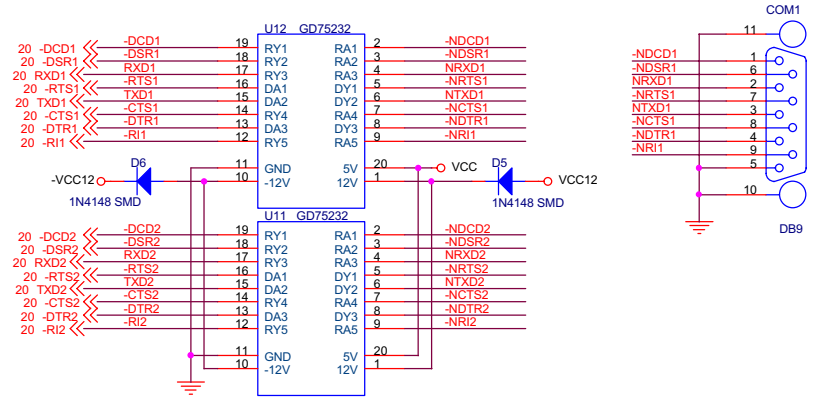
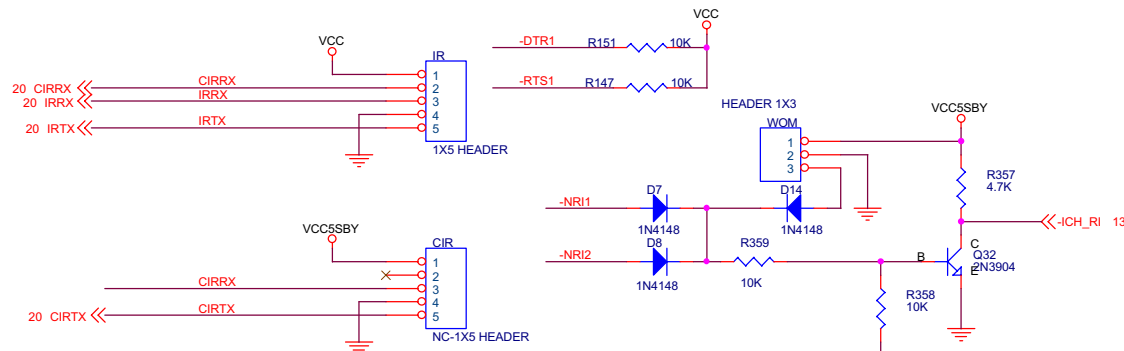
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Size	Document Number	Rev	
B	J615TCF/J615TCS	1	
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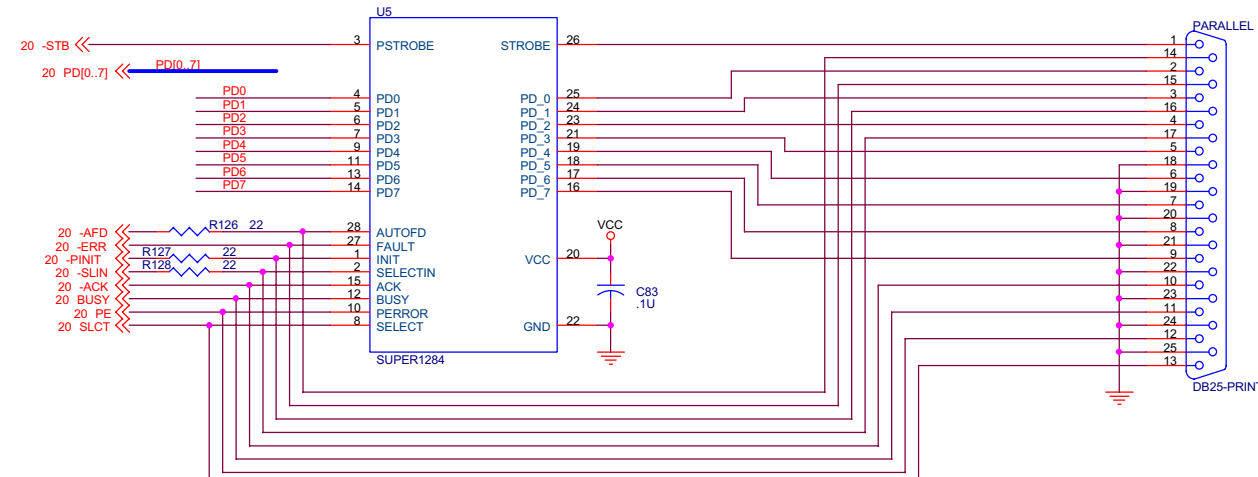


JET WAY INFORMATION		
Title IDE CONNECTORS		
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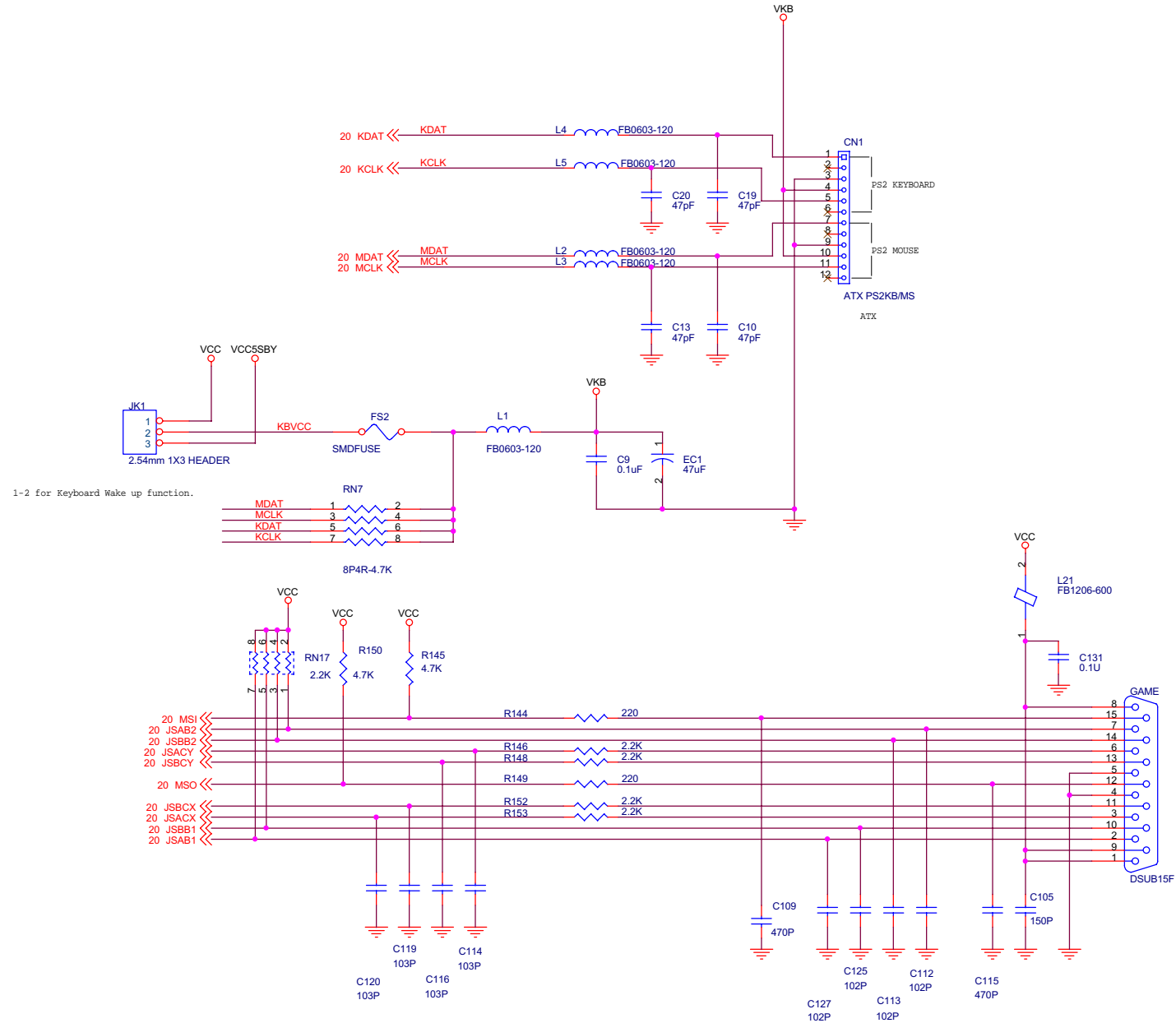
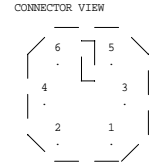
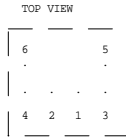


PRT PORT

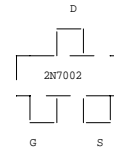


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Size	Document Number	Rev
B	J615TCF/J615TCS	A
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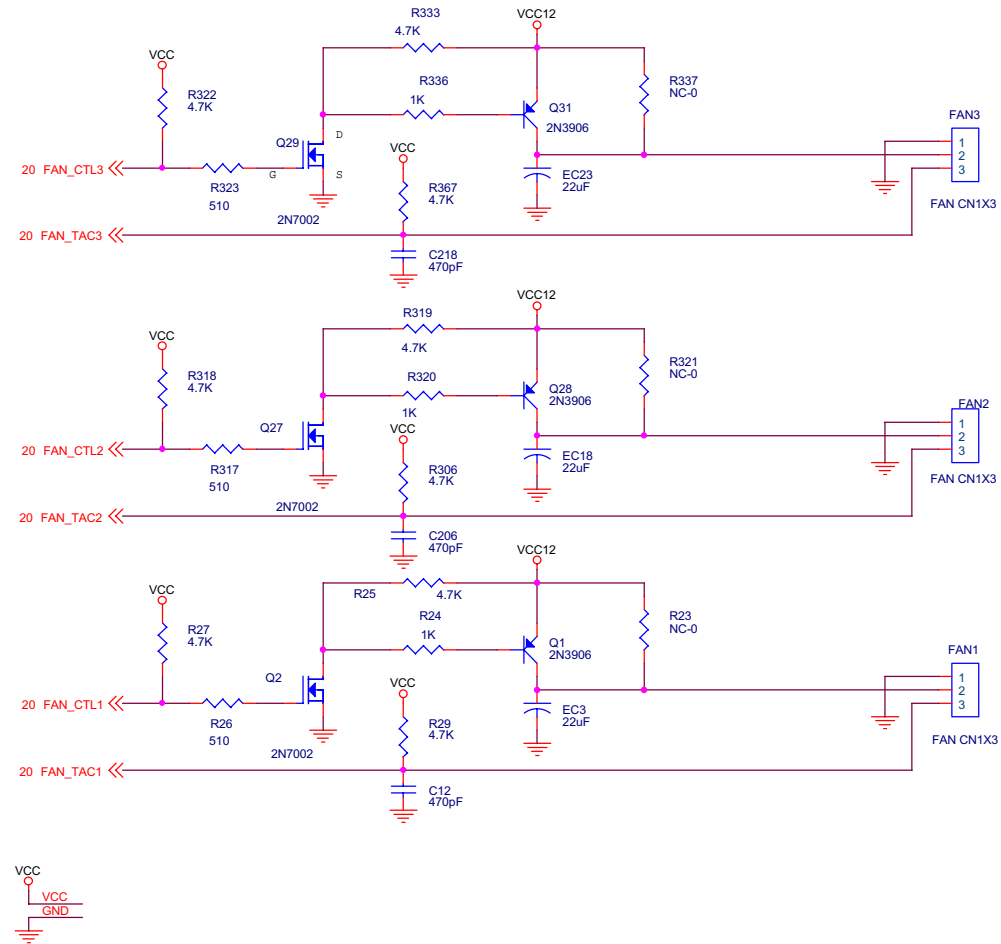
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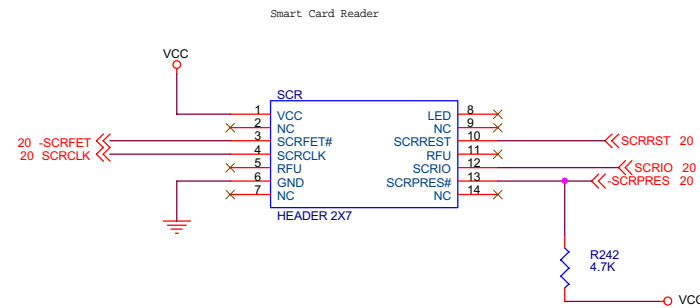
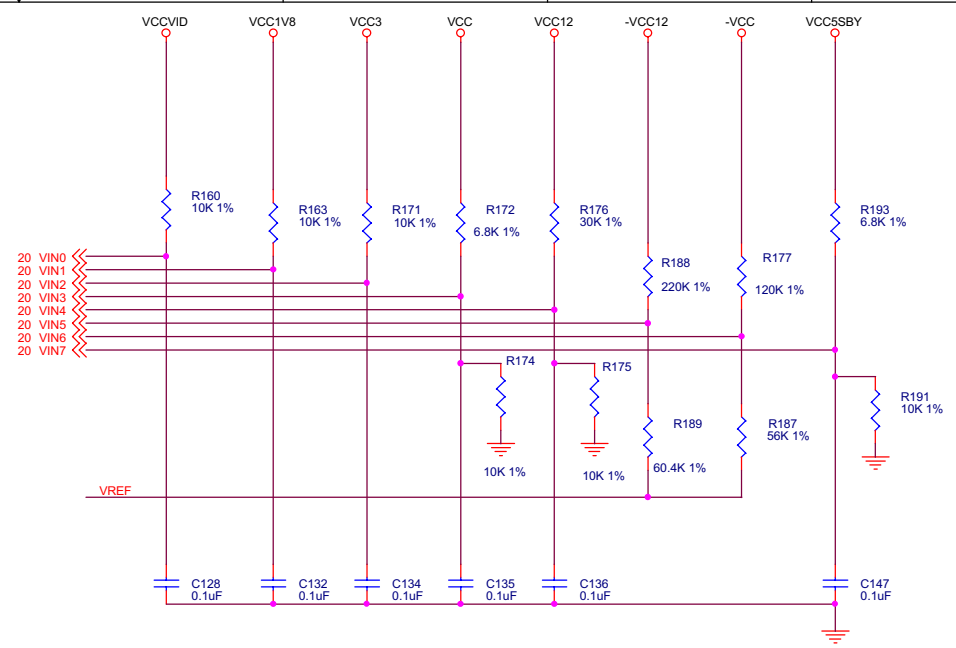
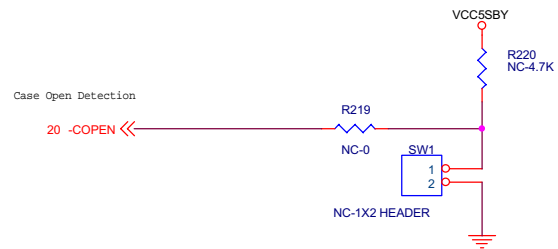
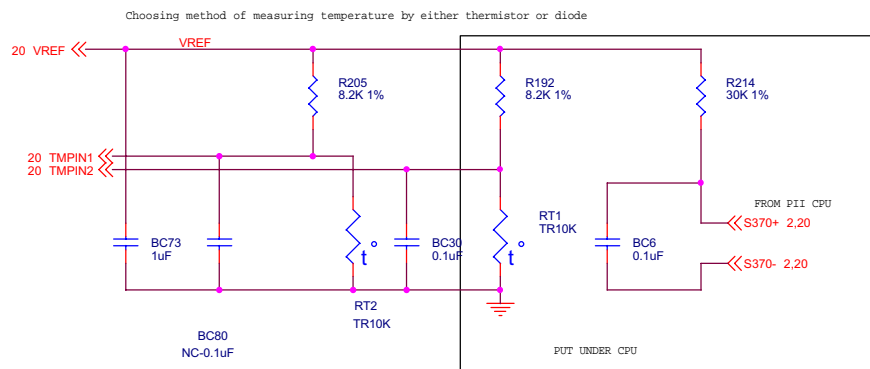
JET WAY INFORMATION		
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Size	Document Number	Rev
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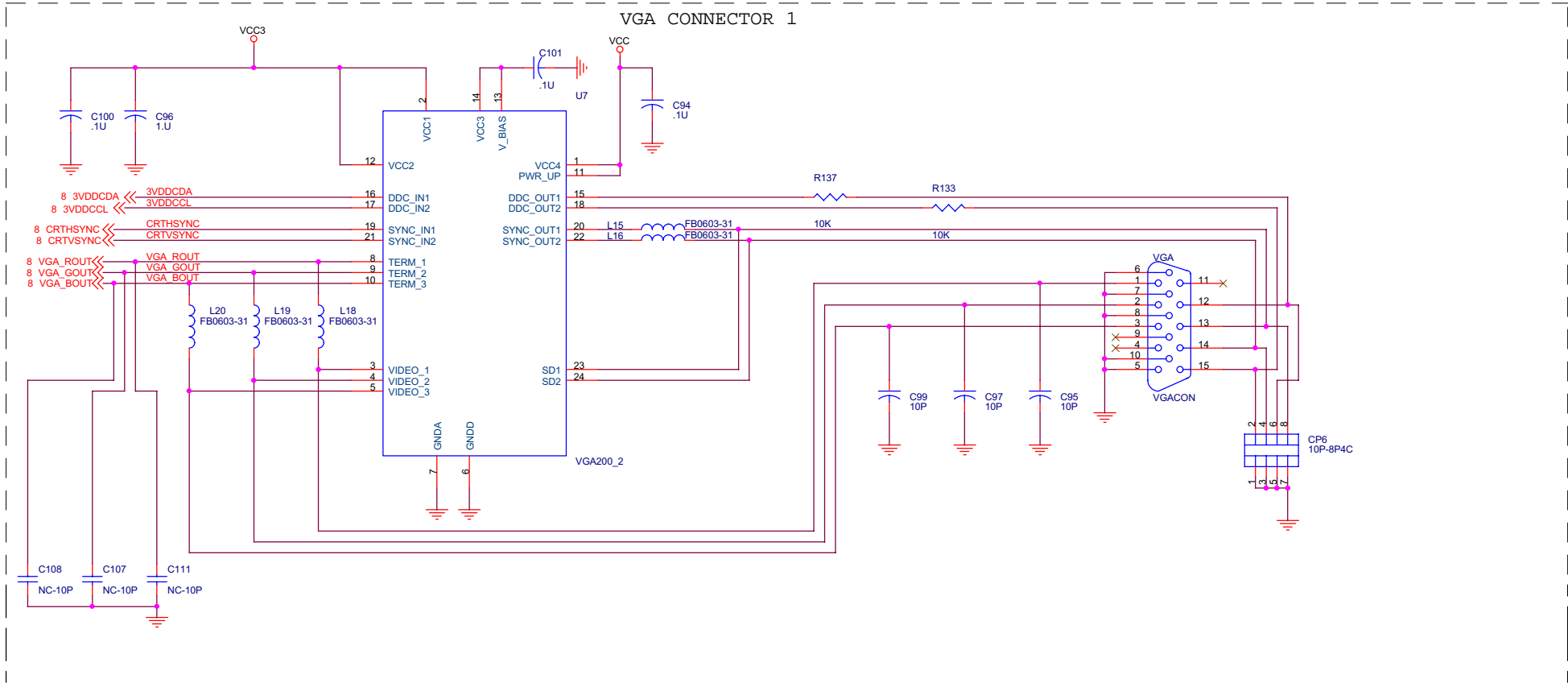
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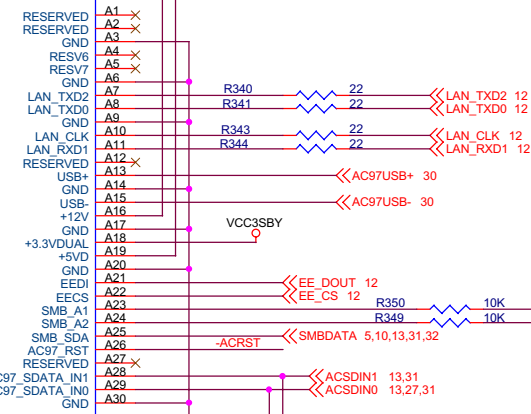
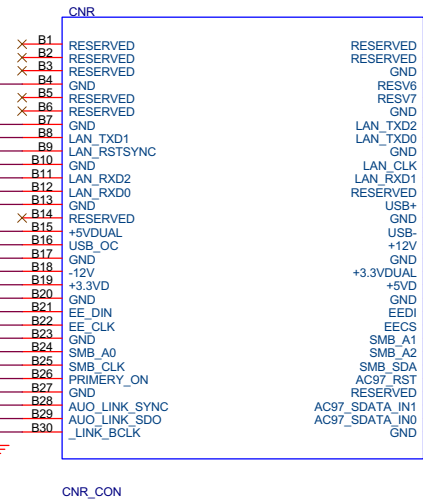
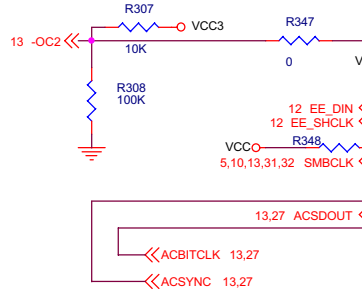
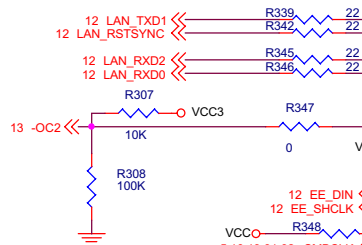
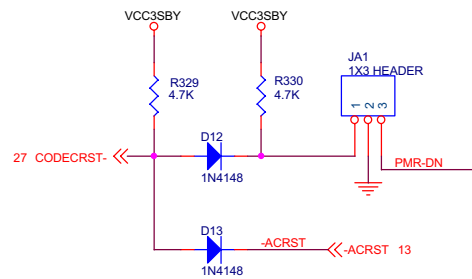
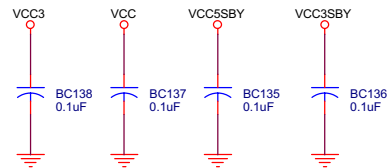
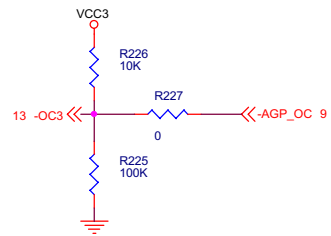
JET WAY INFORMATION		
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Size	Document Number	Rev
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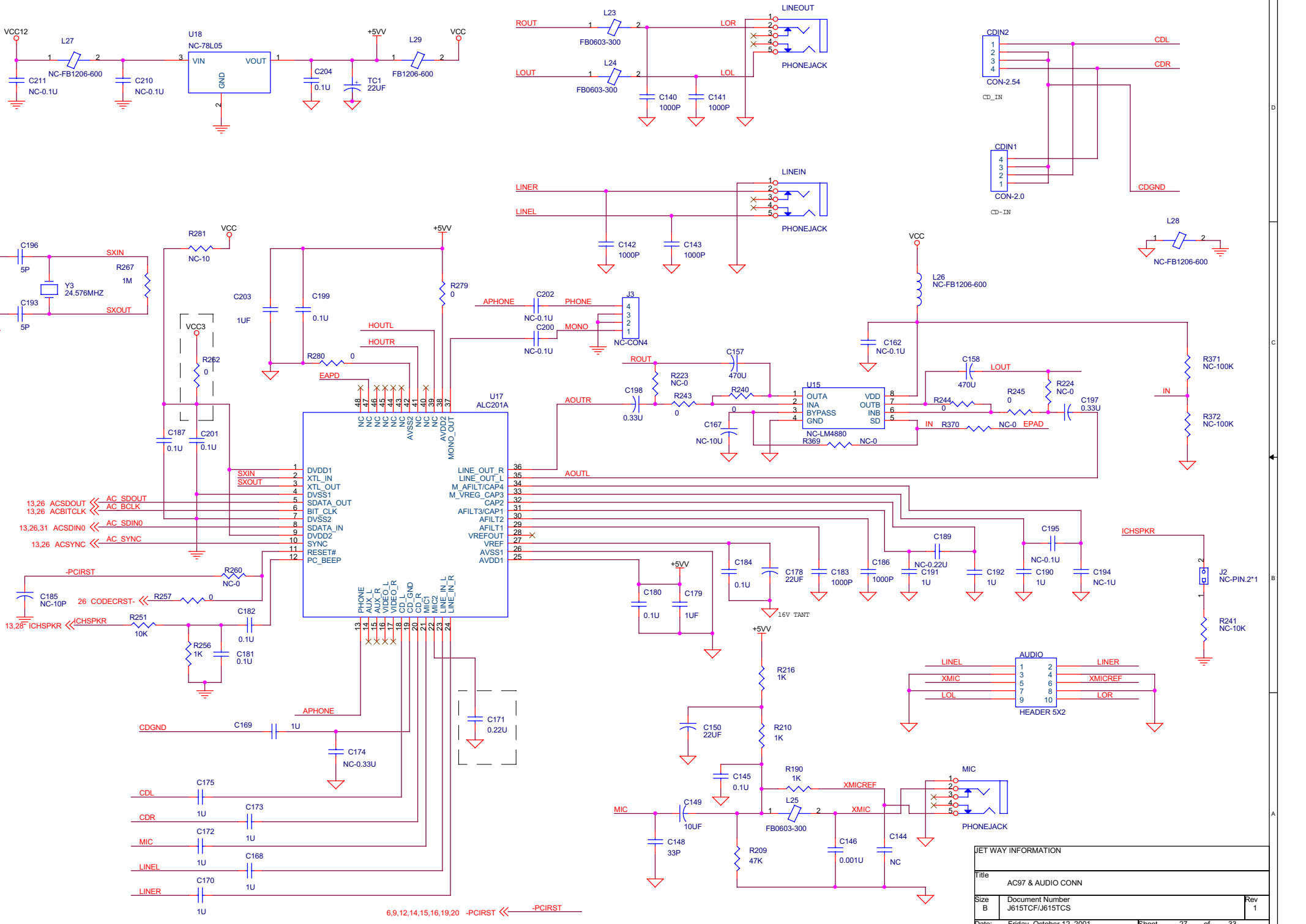
JET WAY INFORMATION		
Title	THERMISTOR, SMART CARD READER	
Size	Document Number	Rev
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JET WAY INFORMATION		
Title VIDEO CONNECTORS		
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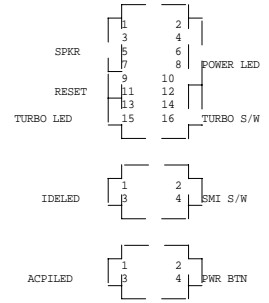
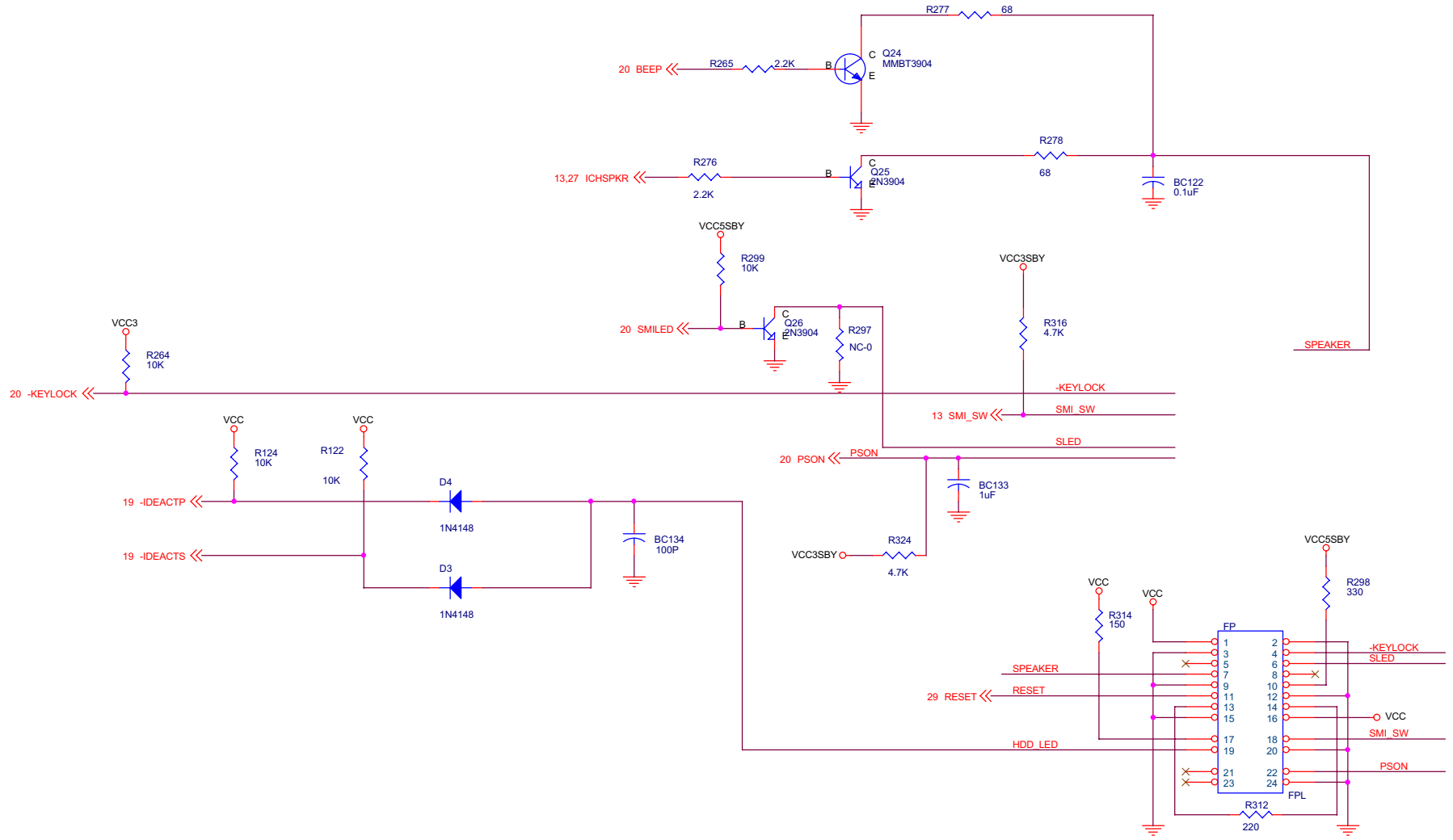


JET WAY INFORMATION			
Title CNR CONNECT			
Size B	Document Number J615TCF/J615TCS		Rev A
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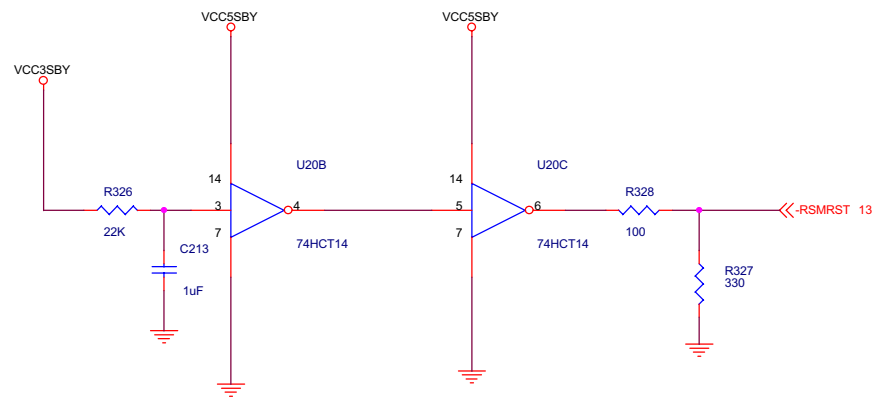
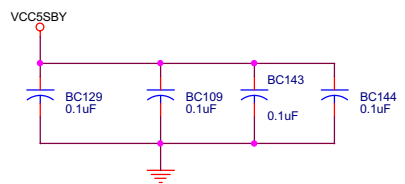
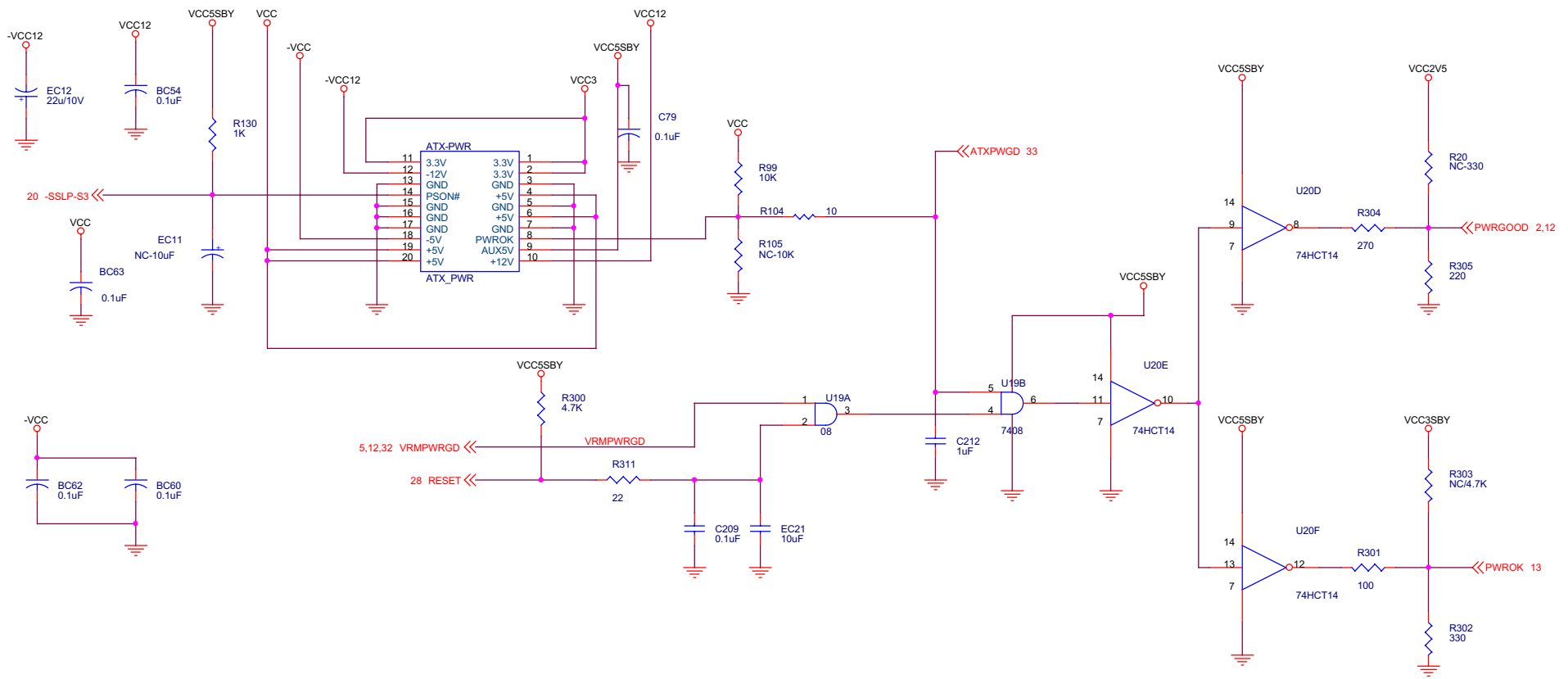


6,9,12,14,15,16,19,20 -PCIRST << -PCIRST

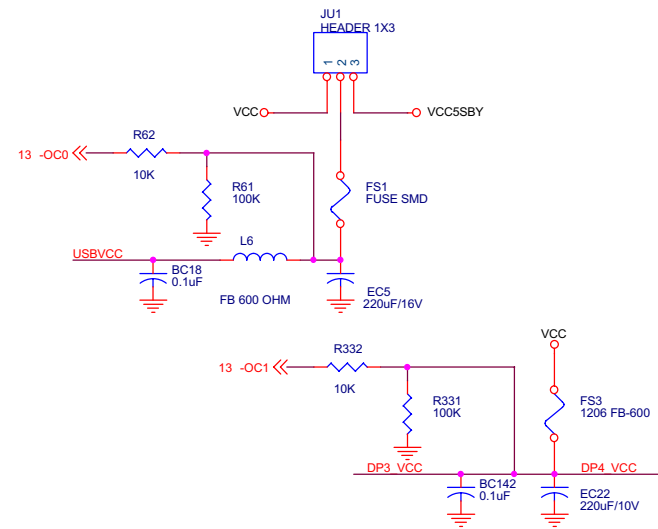
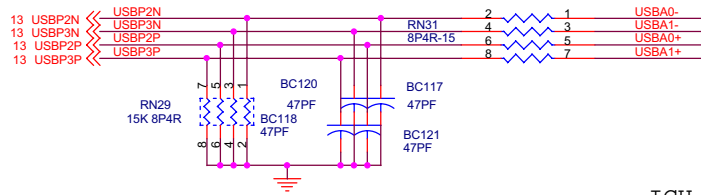
JET WAY INFORMATION		
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Size B	Document Number J615TCF/J615TCS	Rev 1
Date: Friday, October 12, 2001	Sheet 27	of 33



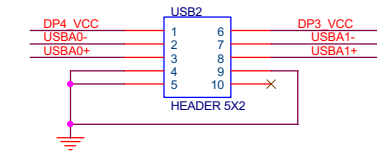
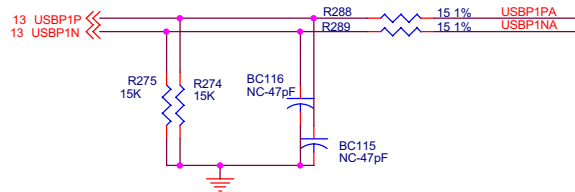
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Size	Document Number	Rev
B	J615TCF/J615TCS	B
Date:	Friday, October 12, 2001	Sheet 28 of 33



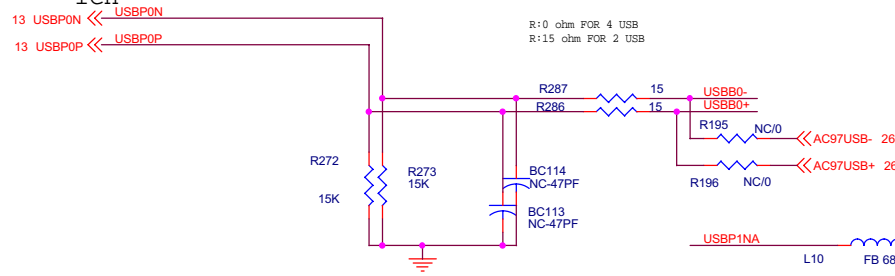
JET WAY INFORMATION		
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Size B	Document Number J615TCF/J615TCS	Rev A
Date: Friday, October 12, 2001	Sheet 29	of 33



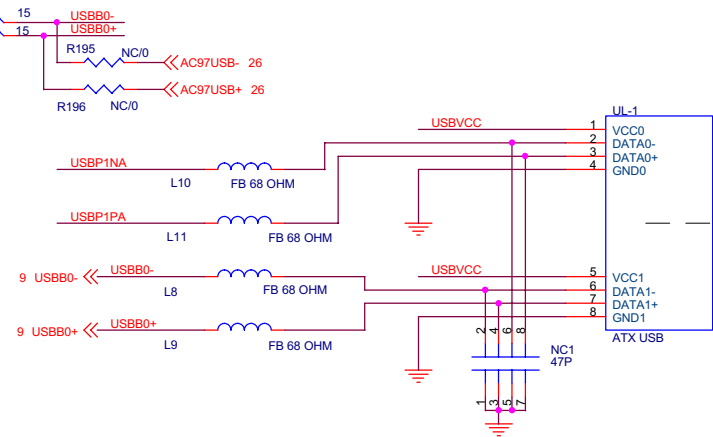
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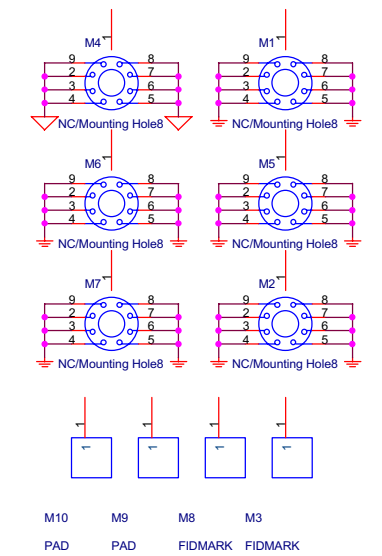
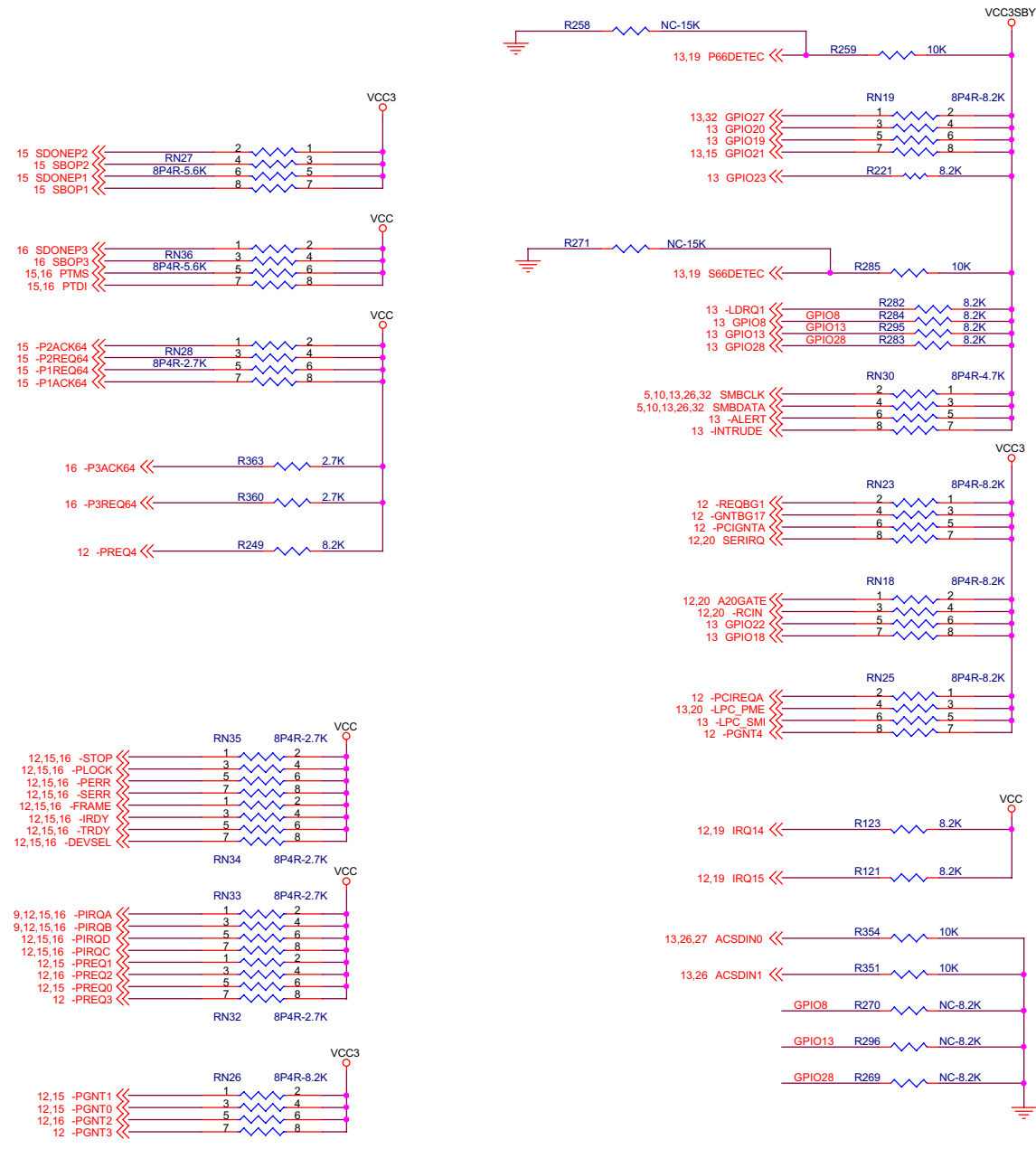
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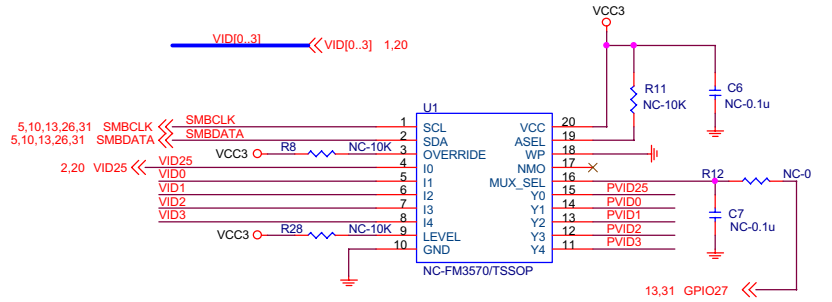
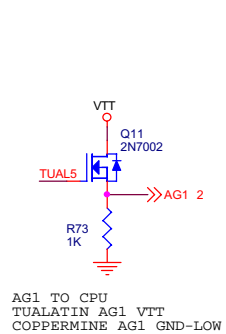
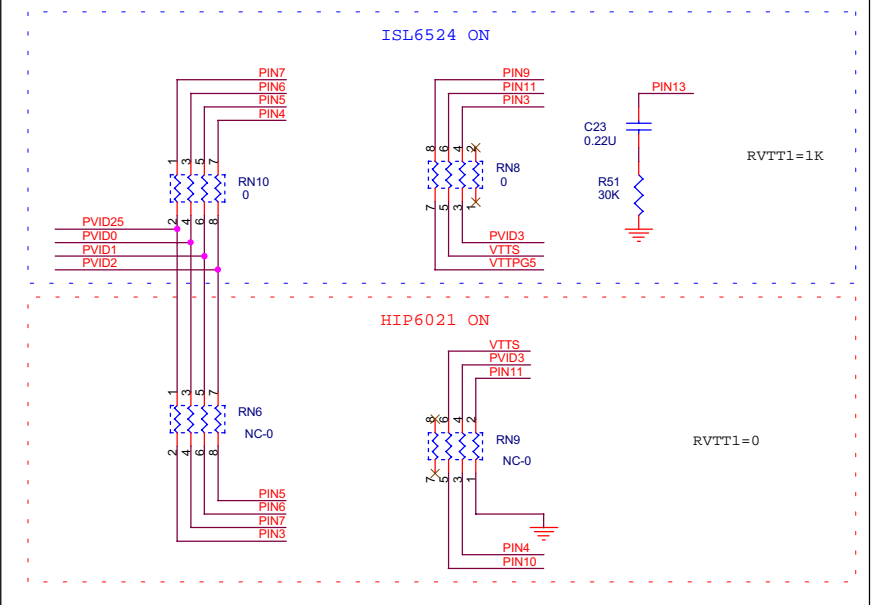
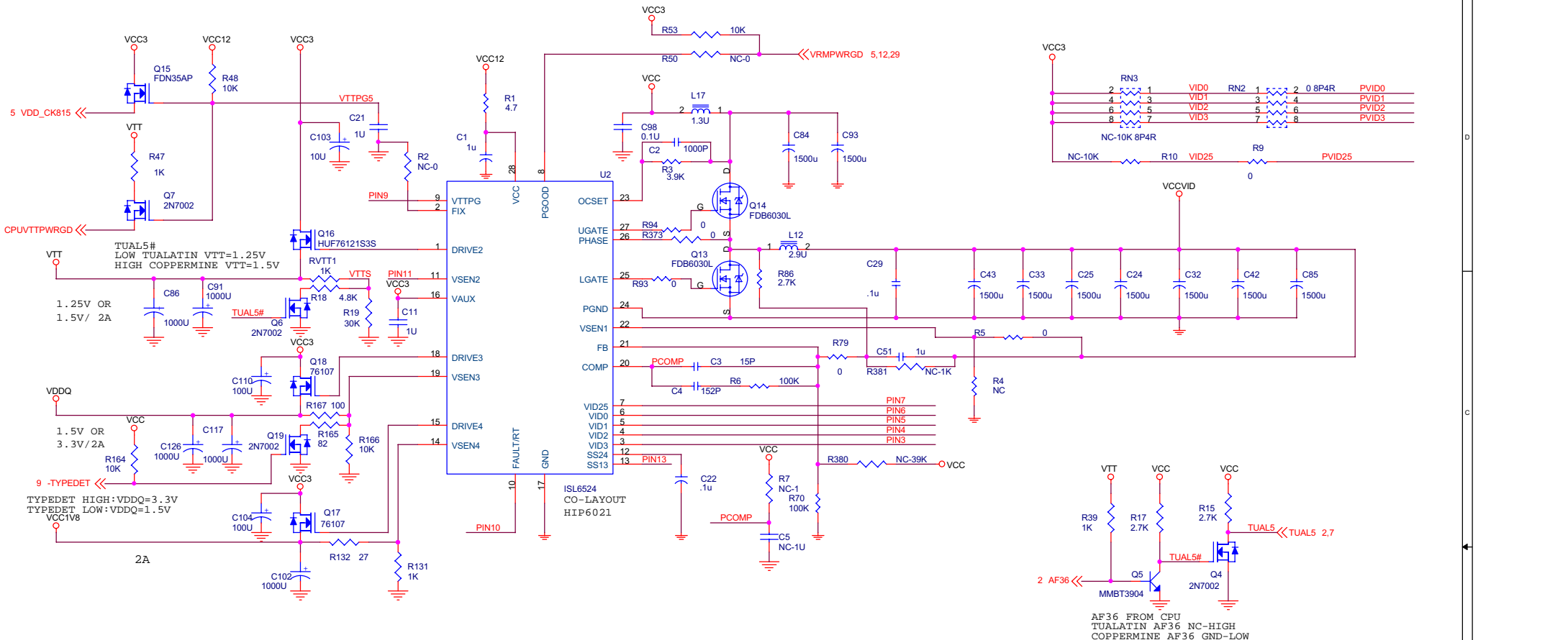
R:0 ohm FOR 4 USB  
 R:15 ohm FOR 2 USB



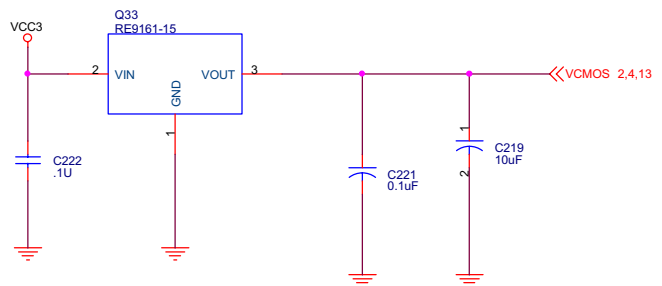
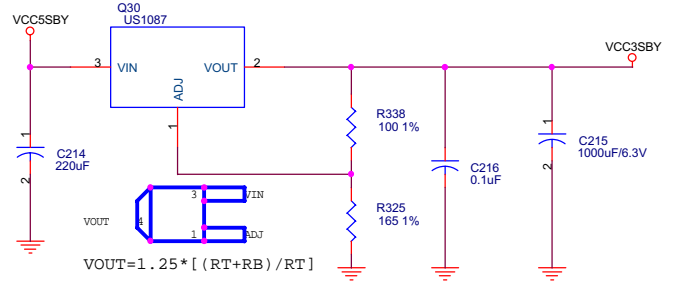
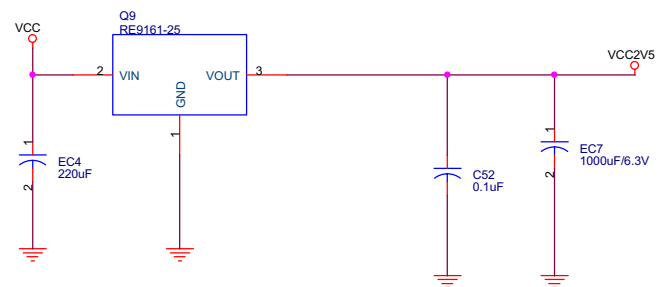
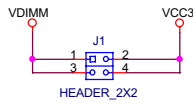
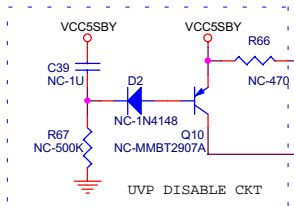
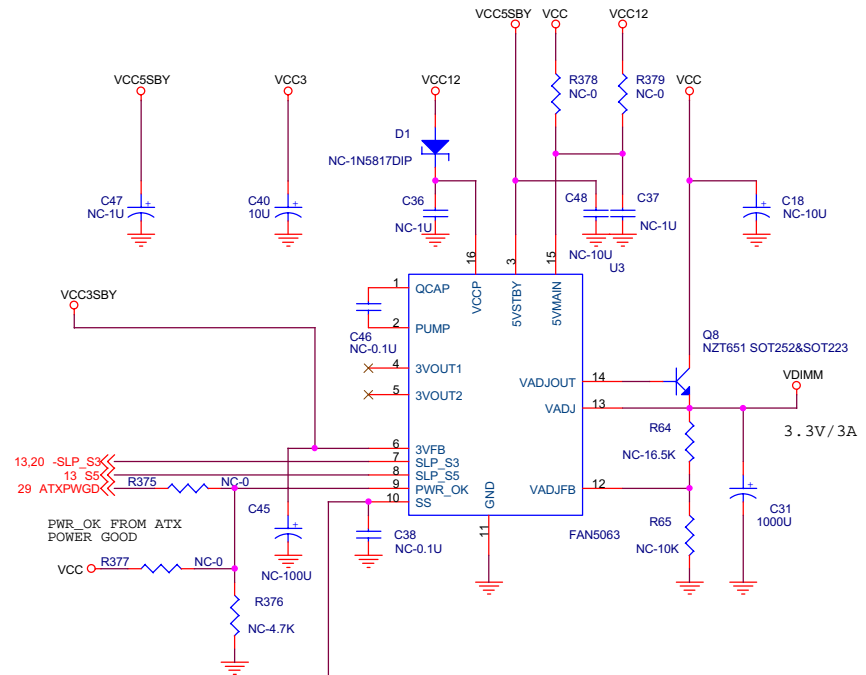
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Size B	Document Number J615TCF/J615TCS	Rev A
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JET WAY INFORMATION			
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JETWAY INFORMATION			
Title DC-DC CONVERTER			
Size C	Document Number J615TCF/J615TCS		Rev 0.1
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JETWAY INFORMATION			
Title DC-DC CONVERTER			
Size	Document Number J615TCF/J615TCS	Rev	0.1
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