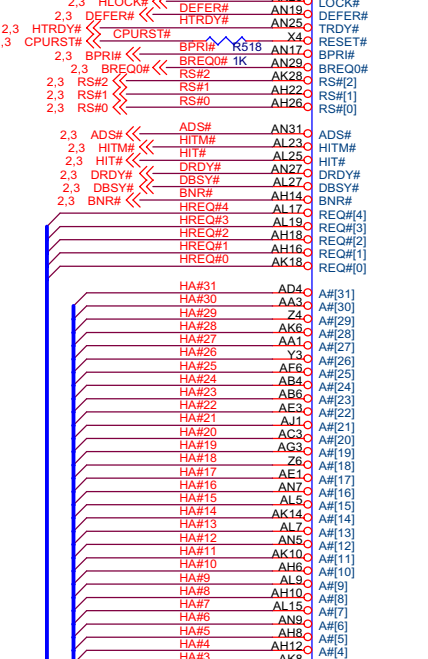
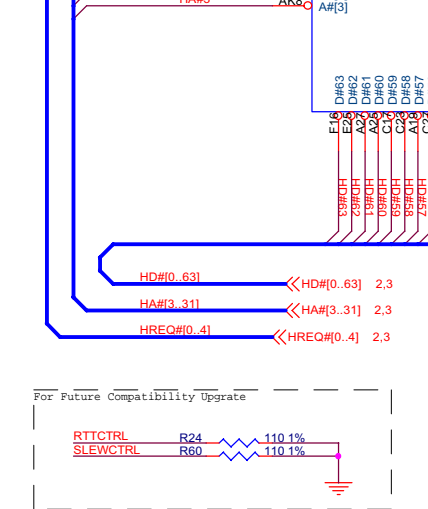


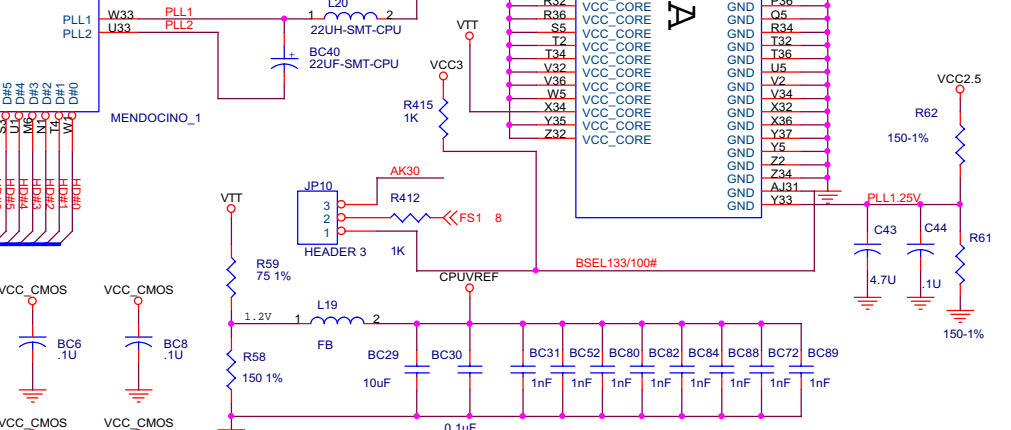
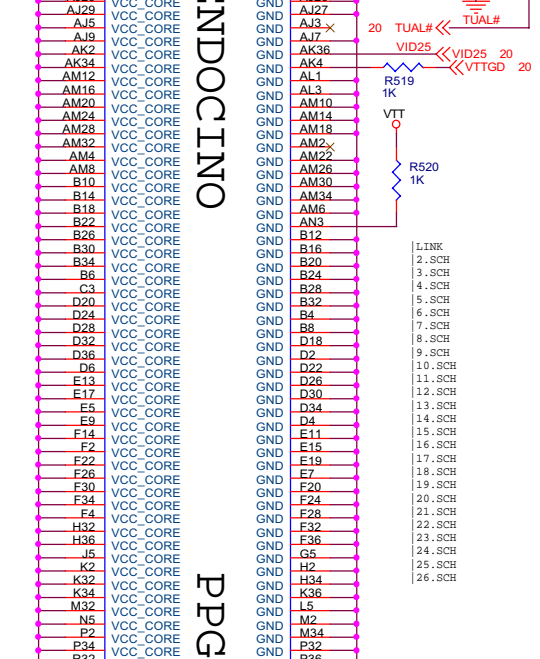
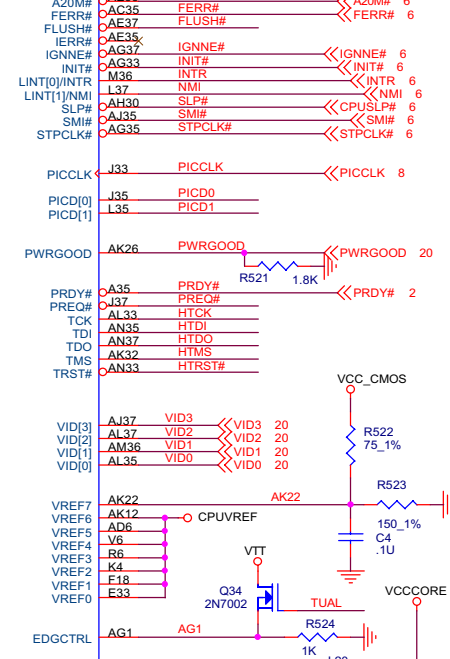
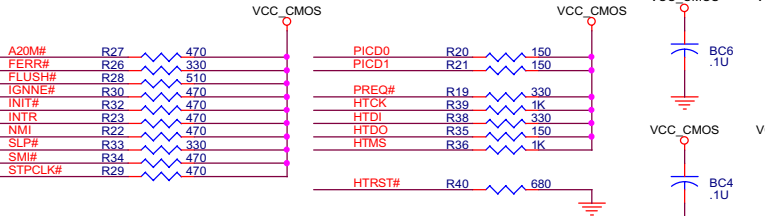
PPGA 370



REQ#	REQ#	REQ#	REQ#	REQ#	VCC_CORE
REQ#4	REQ#3	REQ#2	REQ#1	REQ#0	1.30
1	1	1	0	1	1.35
1	1	0	1	1	1.40
1	1	1	0	0	1.45
1	0	1	1	1	1.50
1	0	1	0	0	1.55
1	0	0	1	1	1.60
1	0	0	0	1	1.65
1	1	0	0	0	1.70
0	1	1	1	1	1.75
0	1	1	0	1	1.80
0	1	0	0	0	1.85
0	0	1	1	1	1.90
0	0	0	1	1	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05

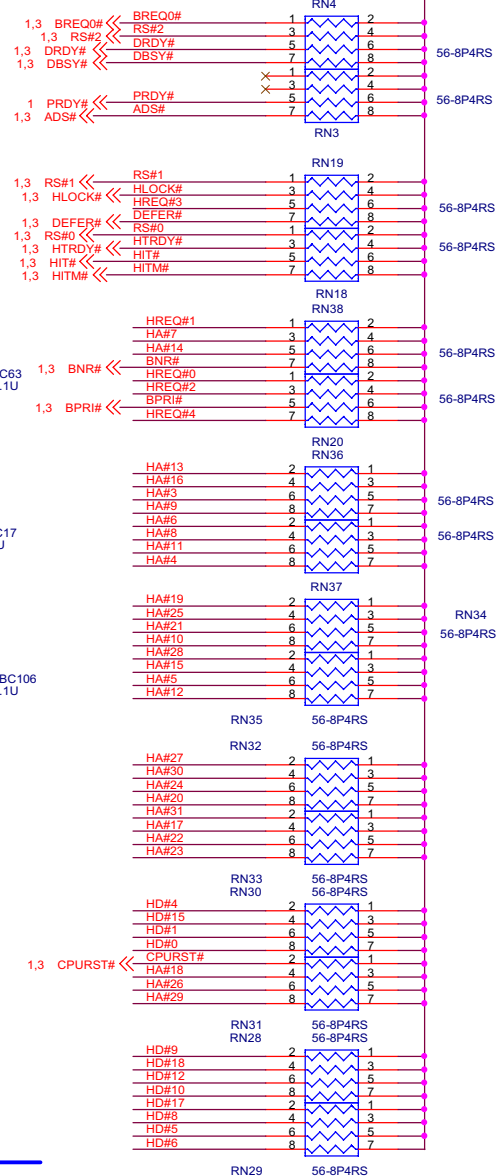
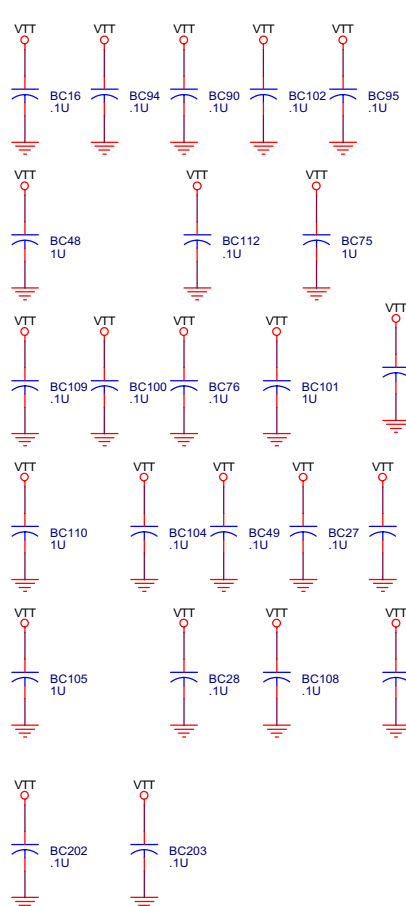


For Cu-256 PU_cmos=150 Ohm



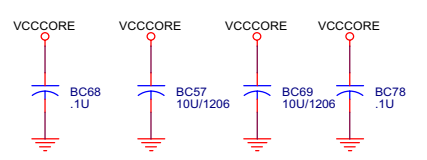
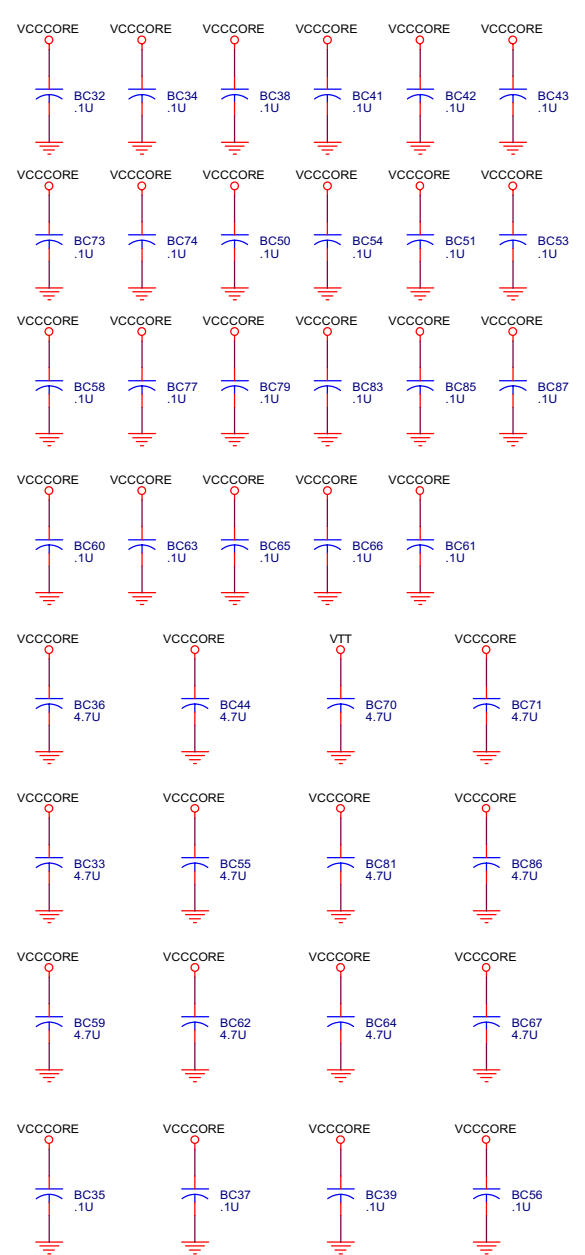
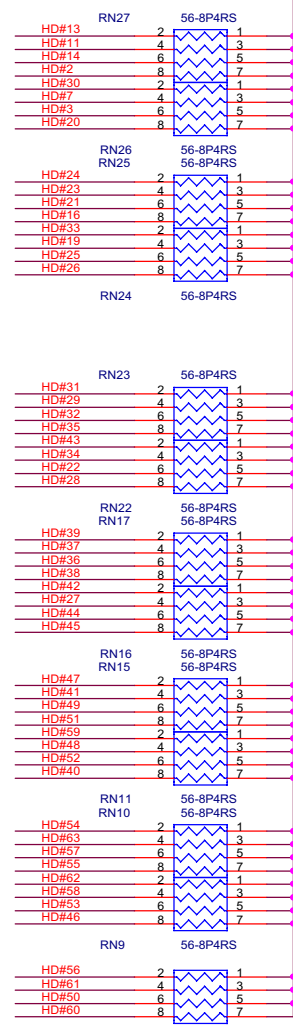
JET WAY INFORMATION		
Title	MENDOCINO PPGA CPU	
Size B	Document Number	Rev
	J-630TCF	3.0
Date:	Monday, October 22, 2001	Sheet 1 of 26

Vtt>50mi1



1,3 HD#[0..63] <<< HD#[0..63]
 1,3 HA#[3..31] <<< HA#[3..31]
 1,3 HREQ#[0..4] <<< HREQ#[0..4]

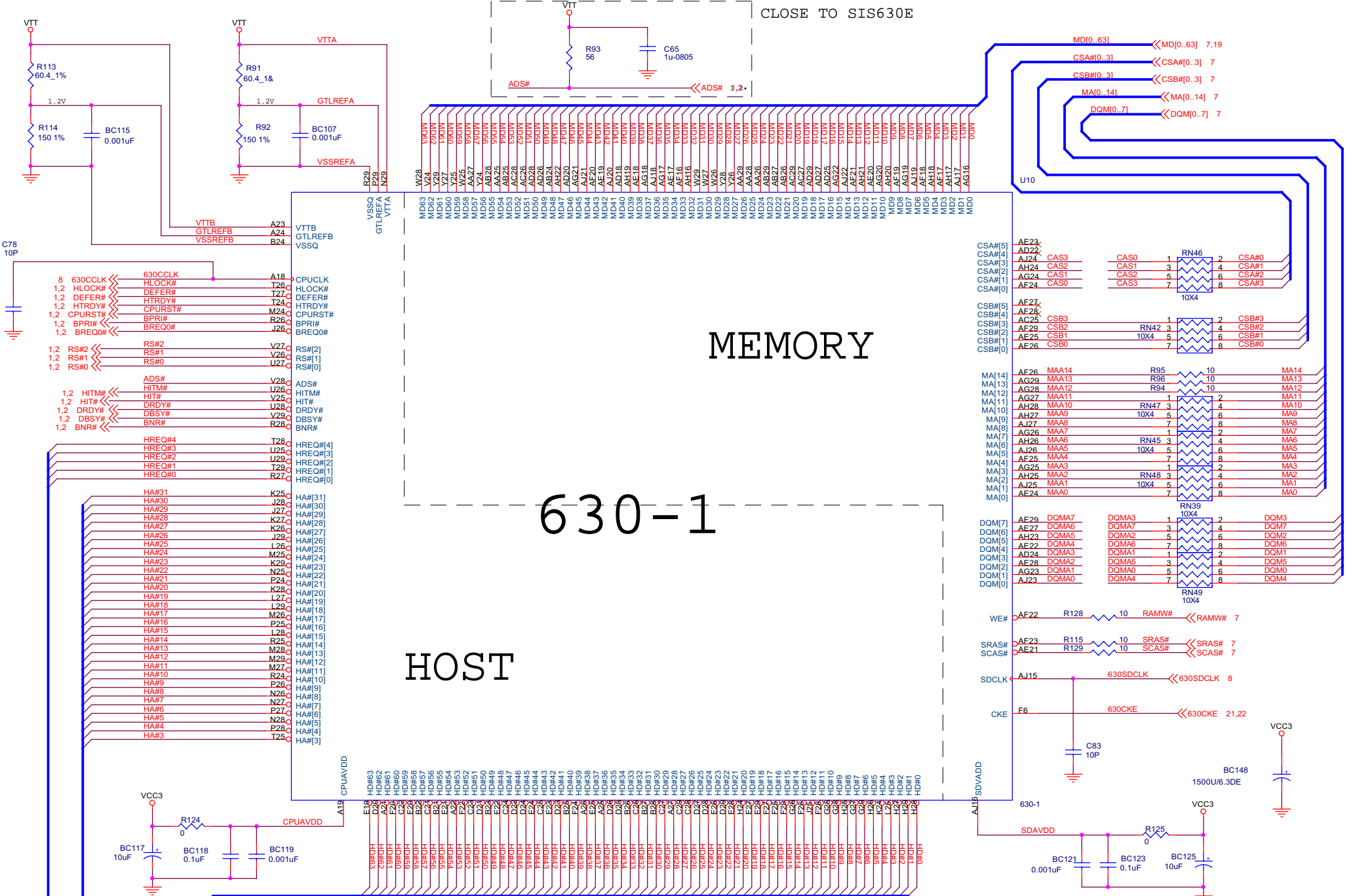
SOCKET 370 RT



NOTE: GTL+ TERMINATION RESISTORS ONLY FOR MENDOCINO PPGA PROCESSOR.

JET WAY INFORMATION		
Title GTL+ TERMINATION RESISTORS		
Size B	Document Number J-630TCF	Rev 3.0
Date: Monday, October 22, 2001	Sheet 2	of 26

CLOSE TO SIS630E

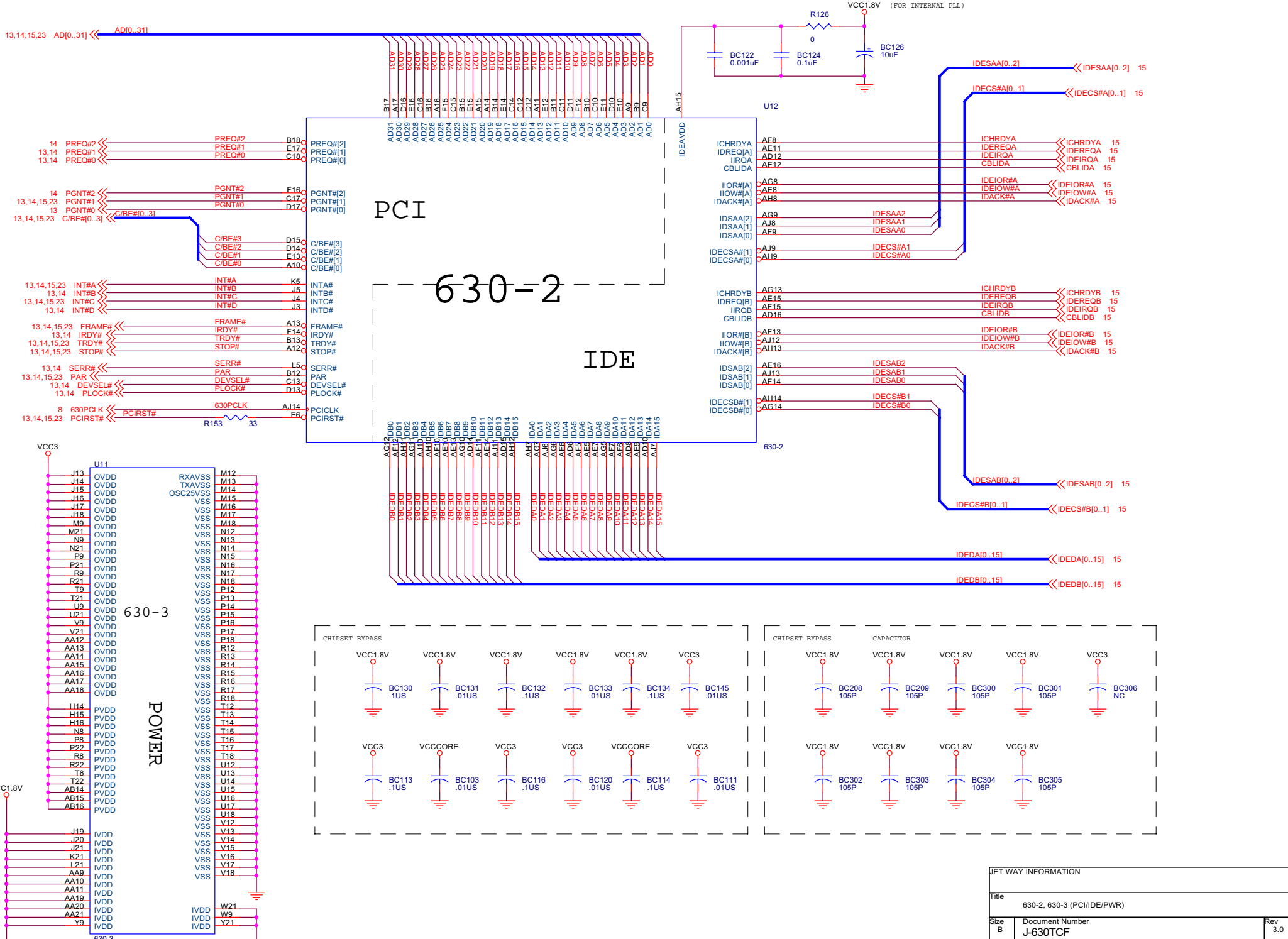


MEMORY

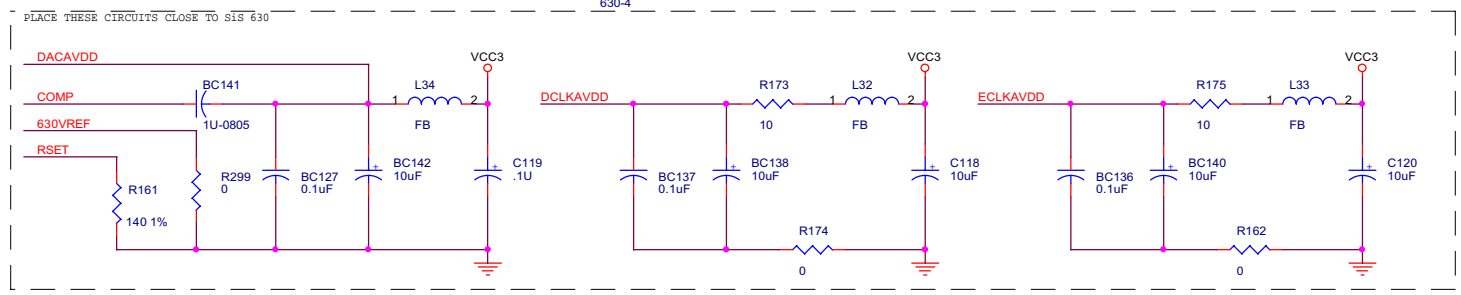
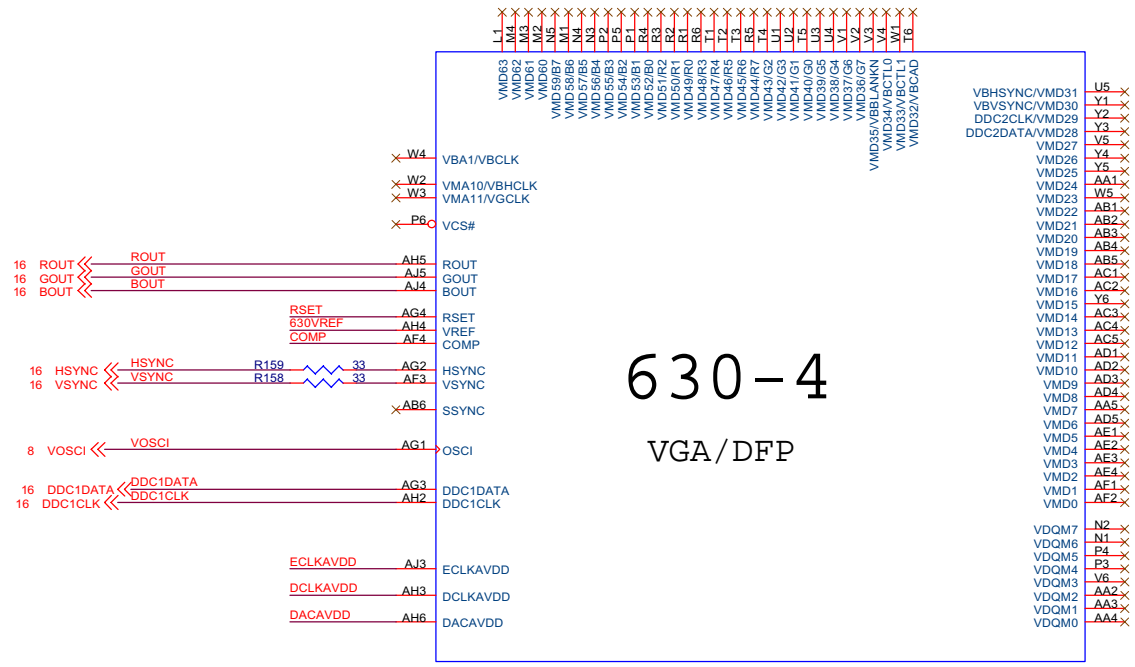
630-1

HOST

JET WAY INFORMATION		
Title	630-1 (HOST/MEMORY)	
Size	Document Number	Rev
B	J-630TCF	3.0
Date:	Monday, October 22, 2001	Sheet 3 of 26

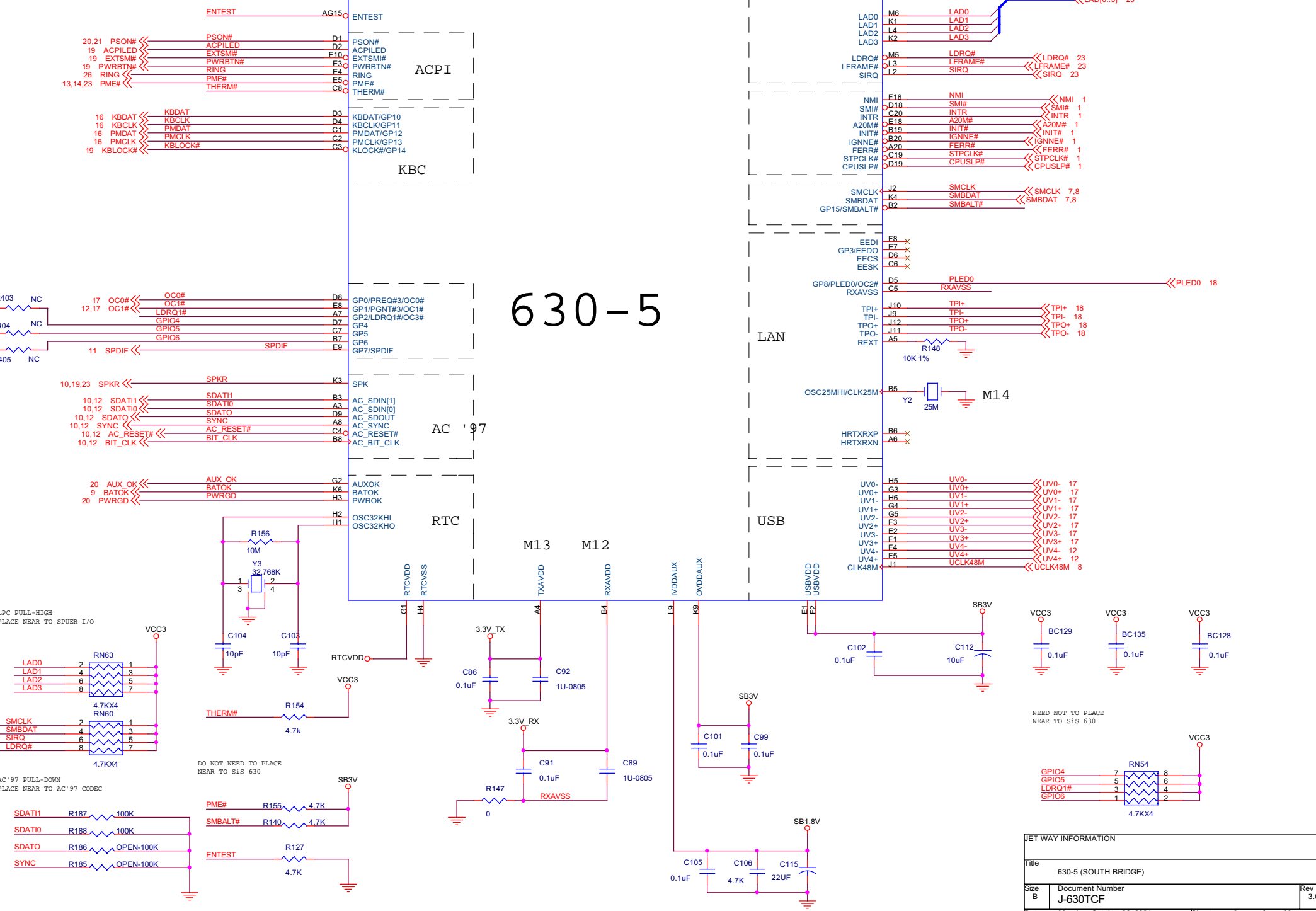


JET WAY INFORMATION		
File	630-2, 630-3 (PCI/IDE/PWR)	
Size	Document Number	Rev
B	J-630TCF	3.0
Date:	Monday, October 22, 2001	Sheet 4 of 26



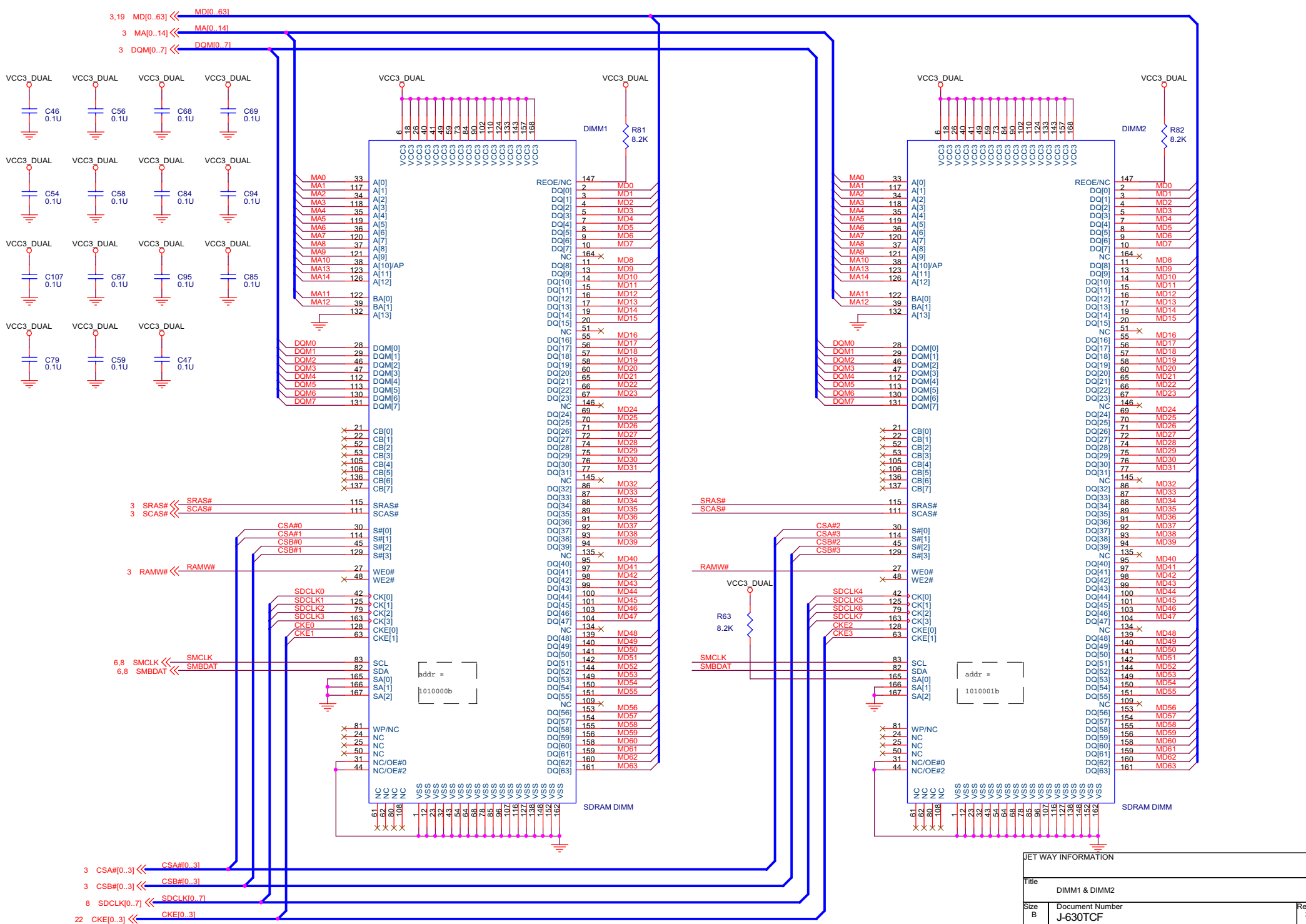
JET WAY INFORMATION		
Title 630-4 (VGA/DFP)		
Size B	Document Number J-630TCF	Rev 3.0
Date: Monday, October 22, 2001	Sheet 5	of 26

U7A
630-5

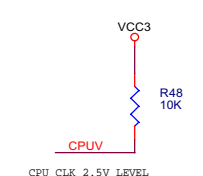
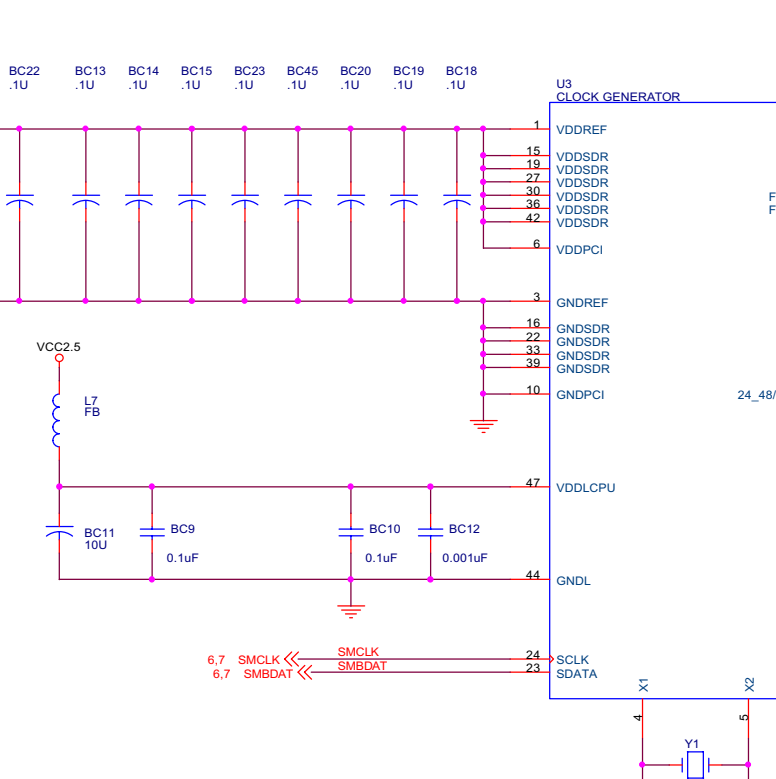
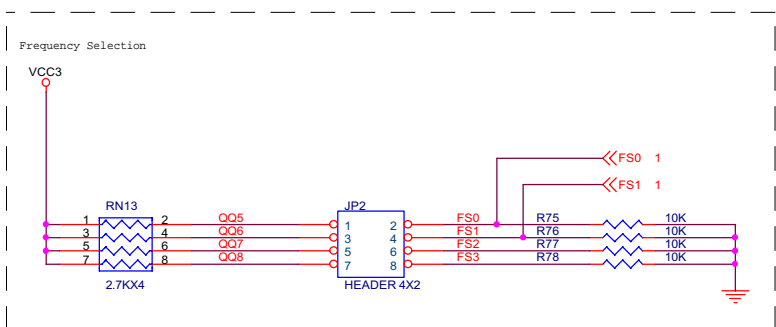


630-5

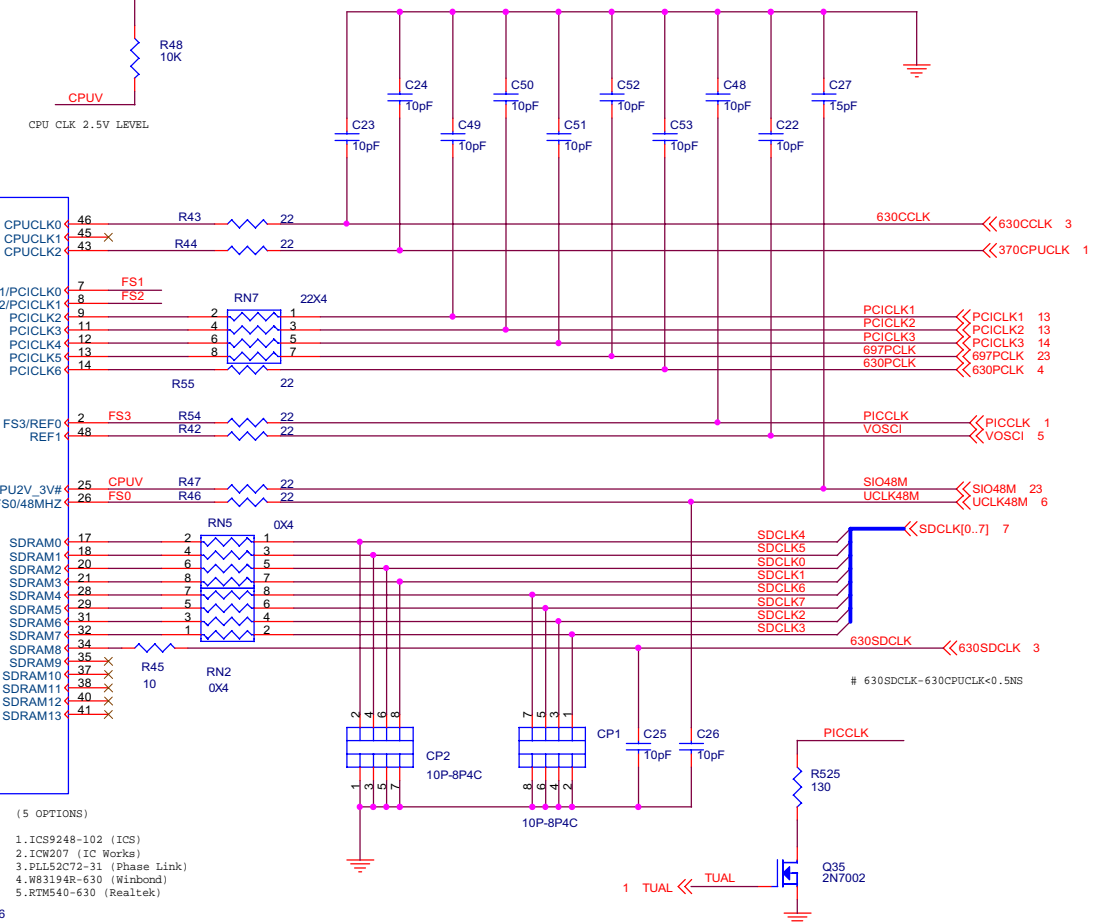
JET WAY INFORMATION		
Title	630-5 (SOUTH BRIDGE)	
Size	Document Number	Rev
B	J-630TCF	3.0
Date:	Monday, October 22, 2001	Sheet 6 of 26



JET WAY INFORMATION		
Title	DIMM1 & DIMM2	
Size	Document Number	Rev
B	J-630TCF	3.0
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@_CLOCK_SPACE >_14_mil



Frequency Selection Table

(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	REF (MHz)
0	0	0	0	66.7	100	33.33	14.318
0	0	0	1	100	100	33.33	14.318
0	0	1	0	150	100	33.33	14.318
0	0	1	1	133	100	33.33	14.318
0	1	0	0	66	133	33.33	14.318
0	1	0	1	100	133	33.33	14.318
0	1	1	0	100	133	33.33	14.318
0	1	1	1	133	133	33.33	14.318
1	0	0	0	66.7	33.33	33.33	14.318
1	0	0	1	83.3	83.3	33.33	14.318
1	0	1	0	90	90	33.33	14.318
1	0	1	1	95	95	33.33	14.318
1	1	0	0	95	126	33.33	14.318
1	1	0	1	112	112	33.33	14.318
1	1	1	0	166	111	33.33	14.318
1	1	1	1	166	166	33.33	14.318

NOTE:
PCICLK<37.5MHz

(5 OPTIONS)

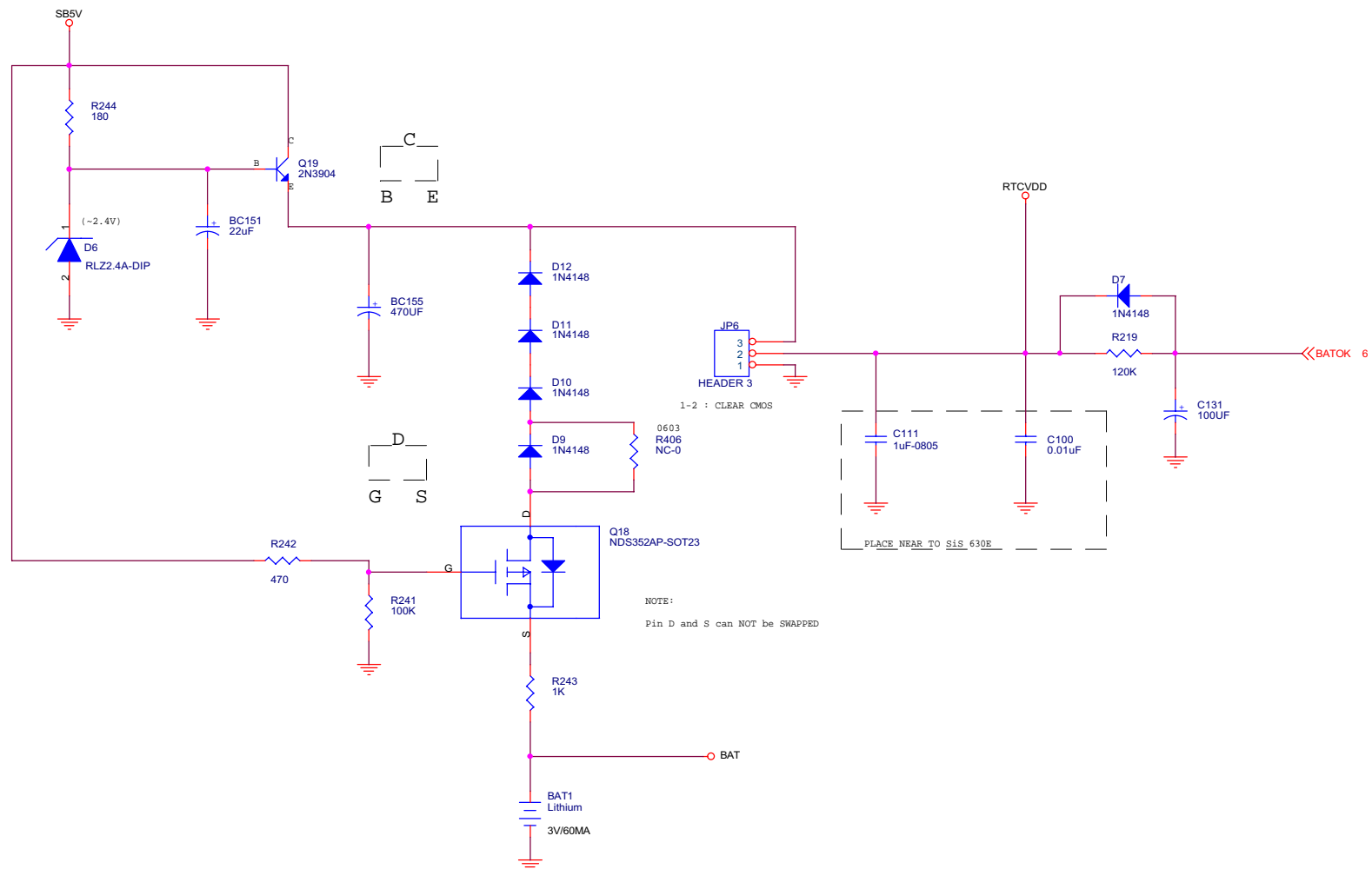
1. ICS9248-102 (ICS)
2. ICN207 (IC Works)
3. PLL52C72-31 (Phase Link)
4. W83194R-630 (Winbond)
5. RTM540-630 (Realtek)

CPU/SDRAM	1-2	3-4	5-6	7-8	JP10	JP11
AUTO	OFF	OFF	OFF	OFF	ON	ON
66/66	OFF	OFF	OFF	ON	OFF	OFF
66/100	OFF	OFF	OFF	OFF	OFF	OFF
100/100	ON	OFF	OFF	OFF	OFF	OFF
100/133	ON	OFF	ON	OFF	OFF	OFF
133/100	ON	ON	OFF	OFF	OFF	OFF
133/133	ON	ON	ON	OFF	OFF	OFF

JET WAY INFORMATION

Title	CLOCK GENERATOR (5 OPTIONS)	
Size	Document Number	Rev
B	J-630TCF	3.0
Date:	Monday, October 22, 2001	Sheet 8 of 26

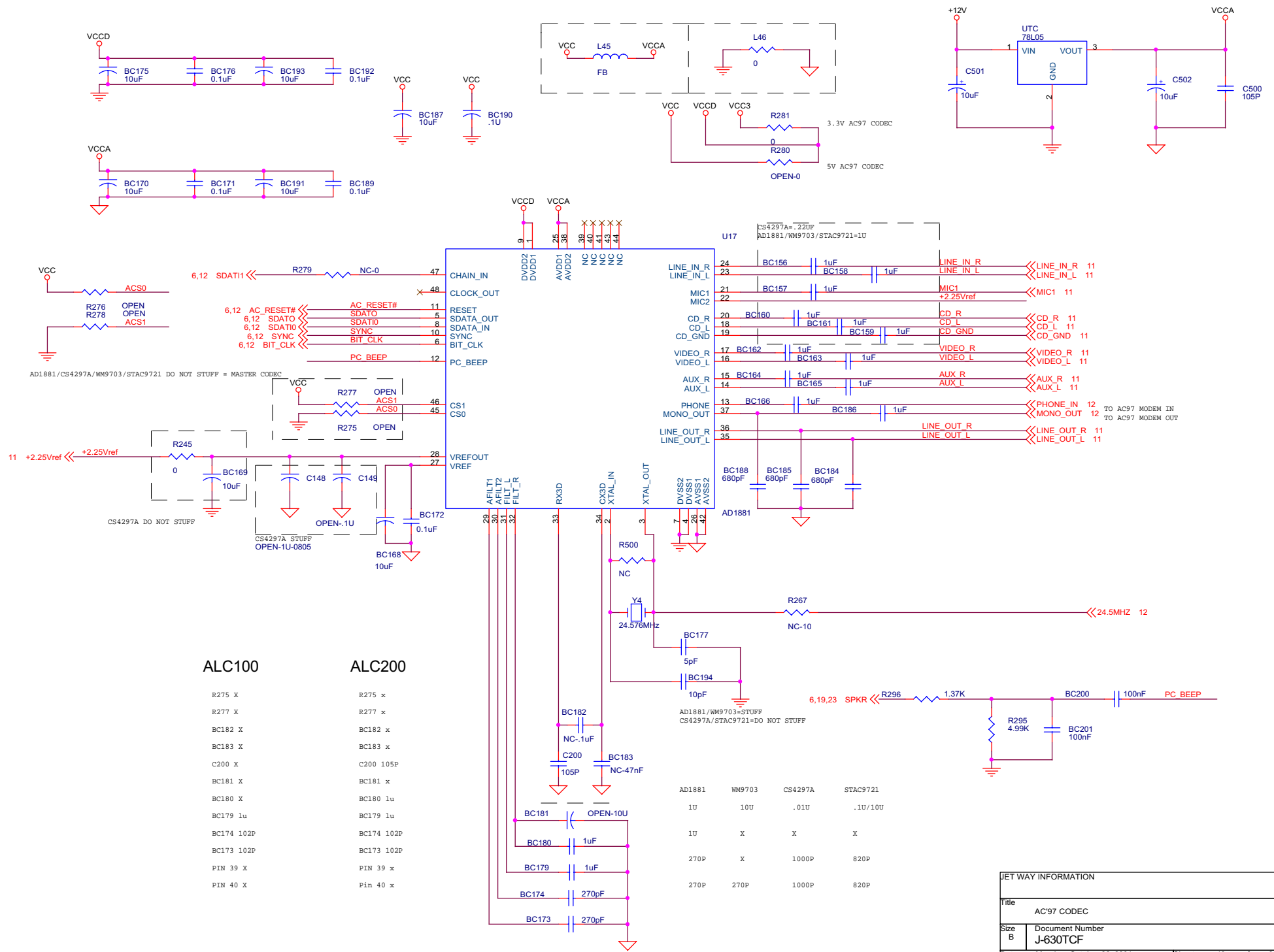
INT. RTC
MUST CLOSE TO CHIP RTCVDD PIN



NOTE:
Pin D and S can NOT be SWAPPED

NOTE:
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ANY ERRORS OR OMISSIONS IN
THESE SCHEMATICS. THIS IS
AN EXAMPLE ONLY.

JET WAY INFORMATION		
Title	RTC	
Size	Document Number	Rev
B	J-630TCF	3.0
Date:	Monday, October 22, 2001	Sheet 9 of 26

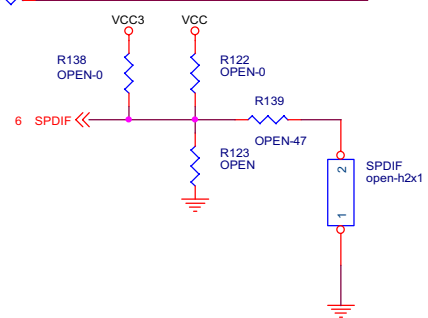
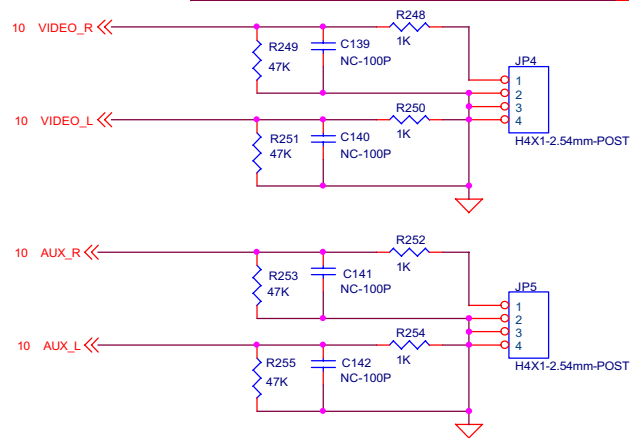
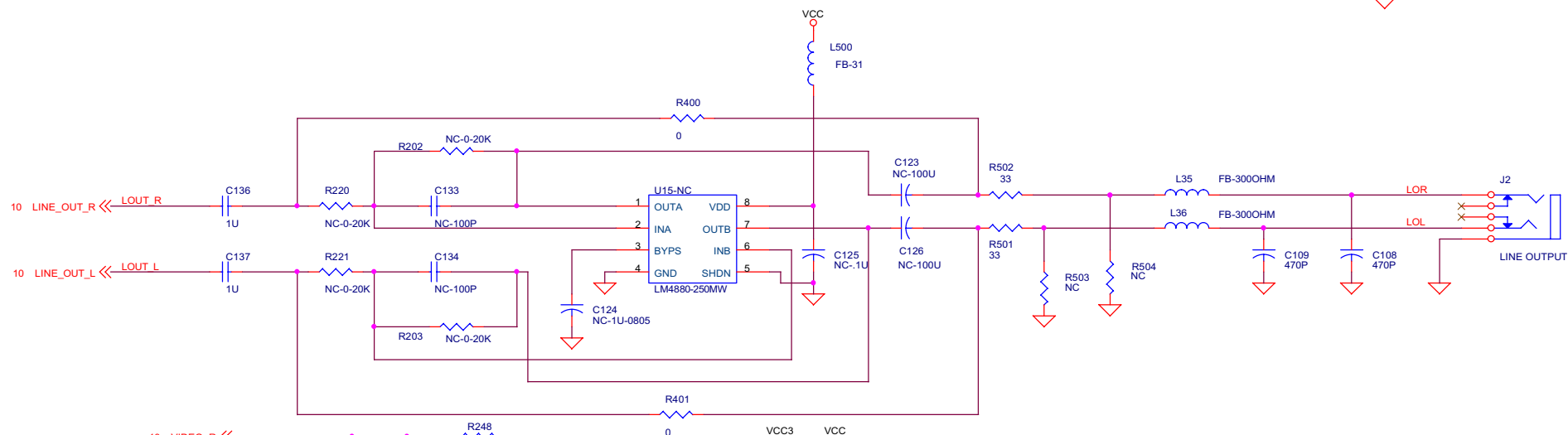
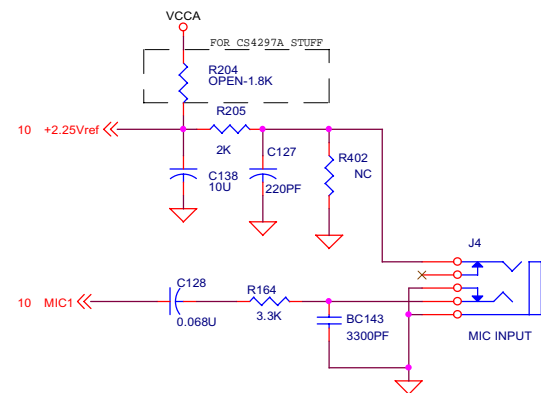
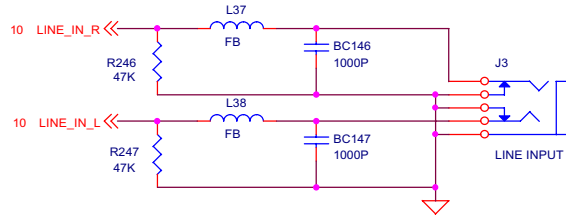
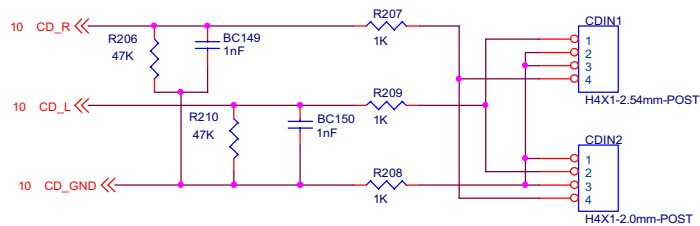


ALC100 ALC200

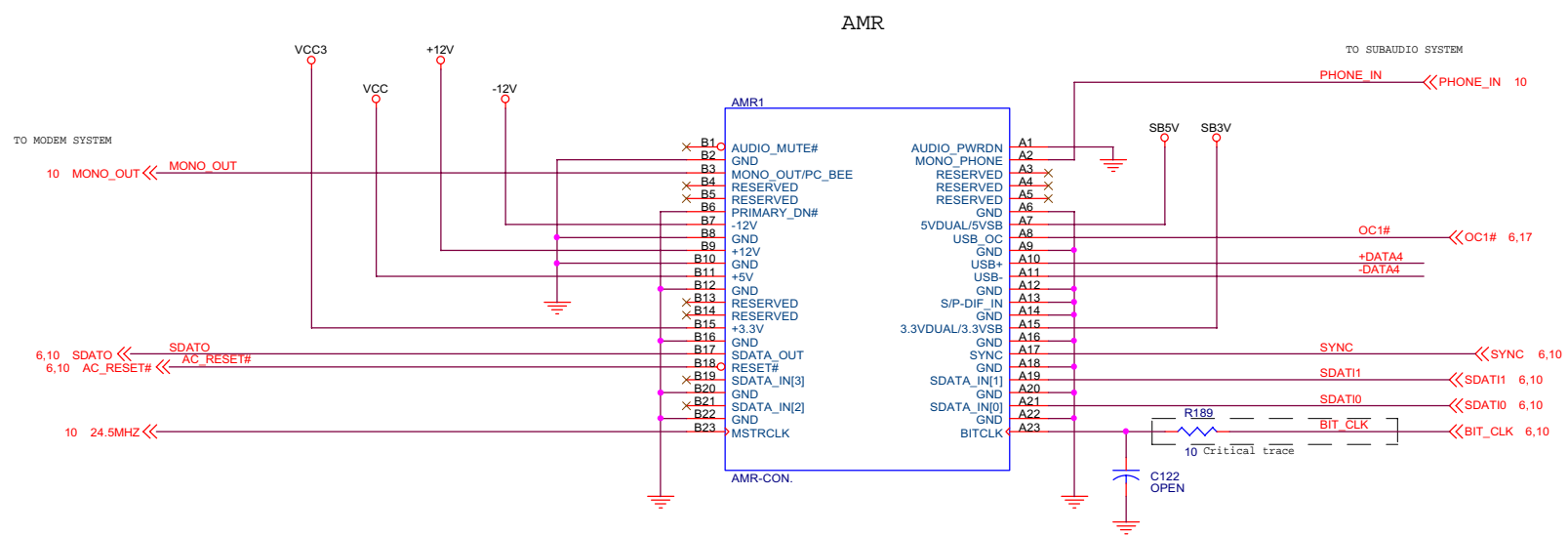
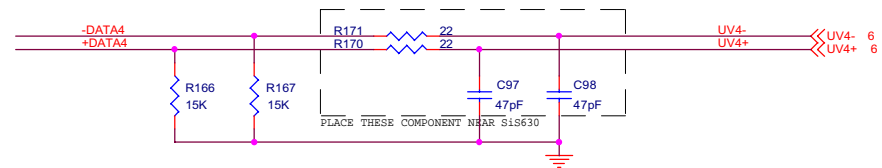
R275	X	R275	x
R277	X	R277	x
BC182	X	BC182	x
BC183	X	BC183	x
C200	X	C200	105P
BC181	X	BC181	x
BC180	X	BC180	1u
BC179	1u	BC179	1u
BC174	102P	BC174	102P
BC173	102P	BC173	102P
PIN 39	X	PIN 39	x
PIN 40	X	PIN 40	x

AD1881	WM9703	CS4297A	STAC9721
1U	10U	.01U	.1U/10U
	X	X	X
270P	X	1000P	820P
270P	270P	1000P	820P

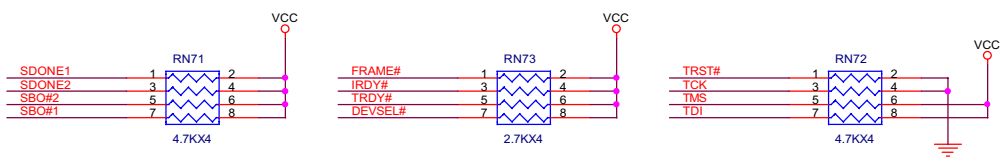
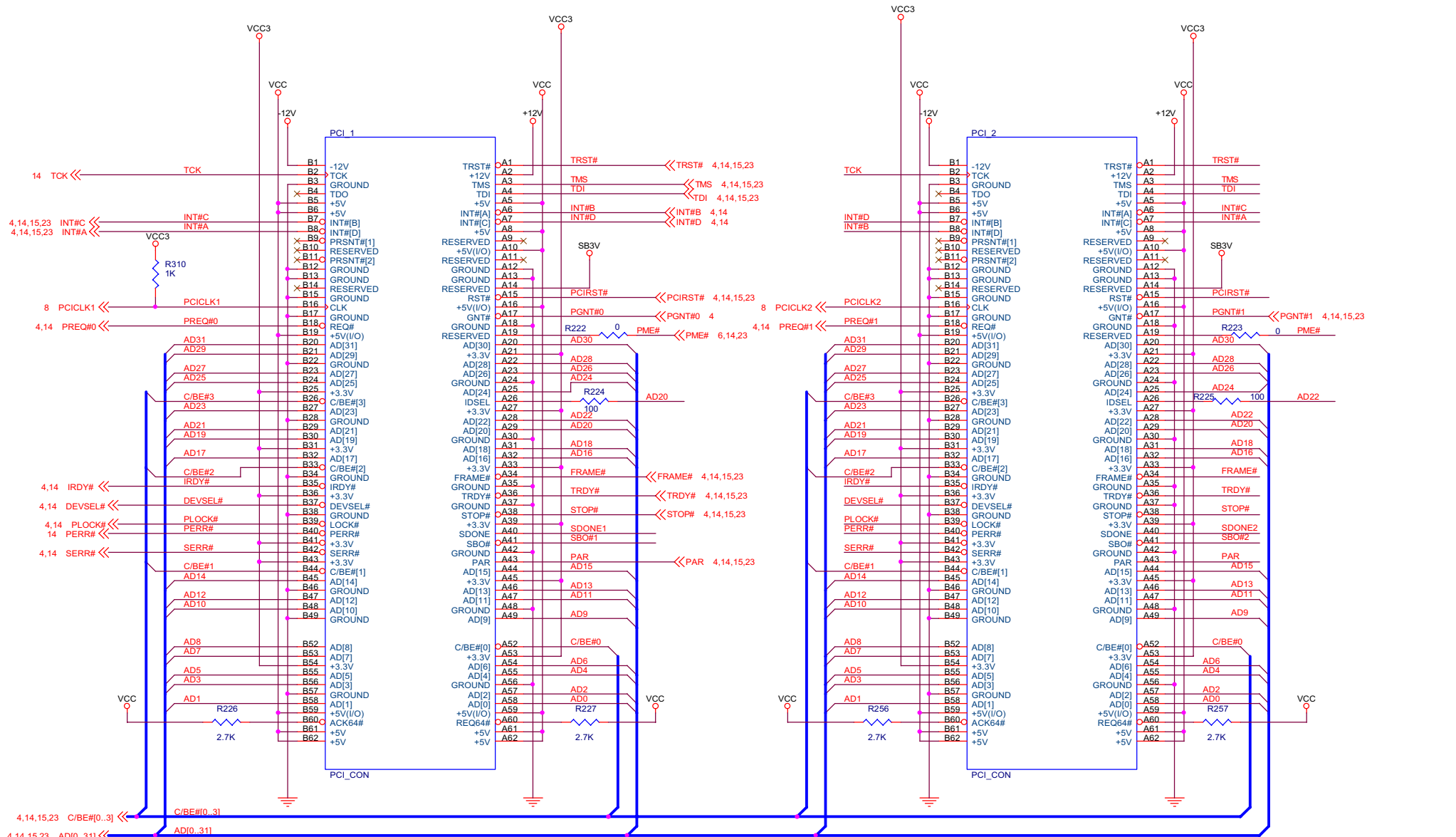
JET WAY INFORMATION		
Title AC'97 CODEC		
Size B	Document Number J-630TCF	Rev 3.0
Date: Monday, October 22, 2001	Sheet 10	of 26



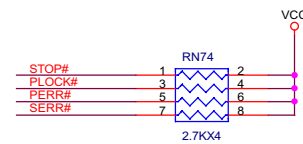
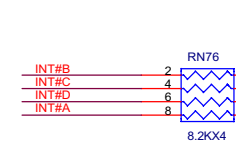
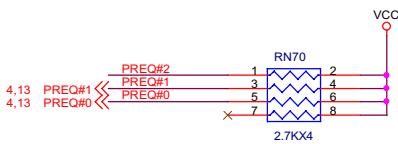
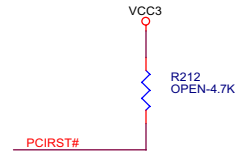
JET WAY INFORMATION		
Title AUDIO ANALOGUE IN/OUT		
Size B	Document Number J-630TCF	Rev 3.0
Date: Monday, October 22, 2001	Sheet 11	of 26



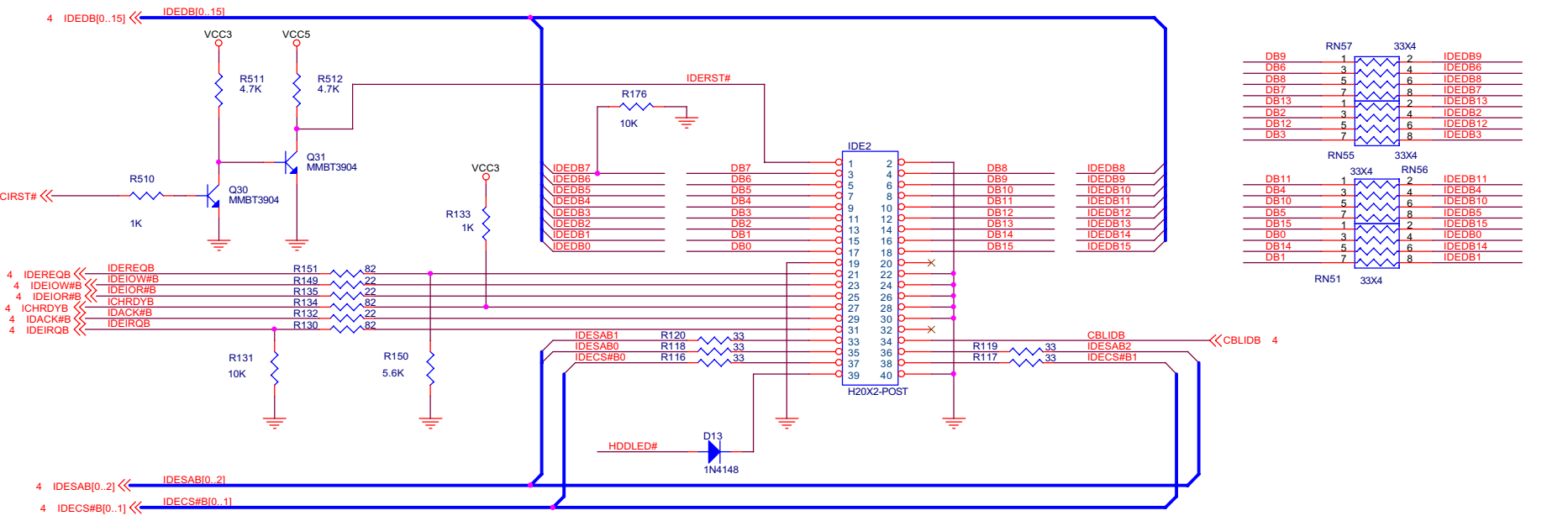
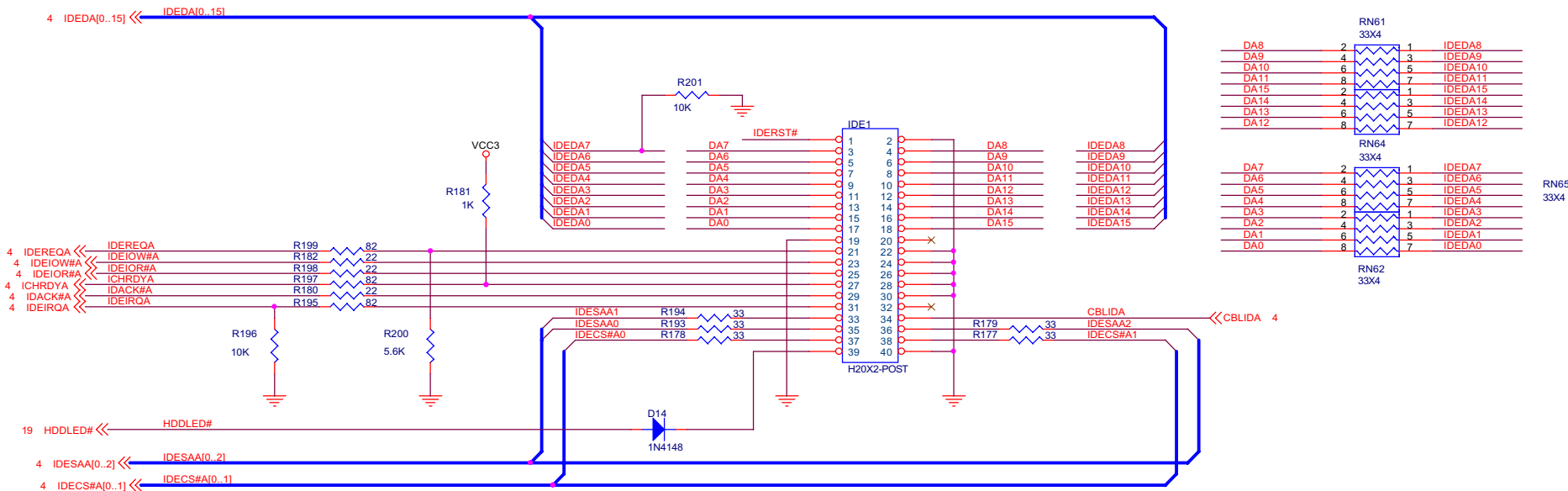
JET WAY INFORMATION			
Title AUDIO/MODEM RISER			
Size B	Document Number J-630TCF		Rev 3.0
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JET WAY INFORMATION		
Title	PCI CONNECTOR 1 & 2	
Size	Document Number	Rev
B	J-630TCF	3.0
Date:	Monday, October 22, 2001	Sheet 13 of 26

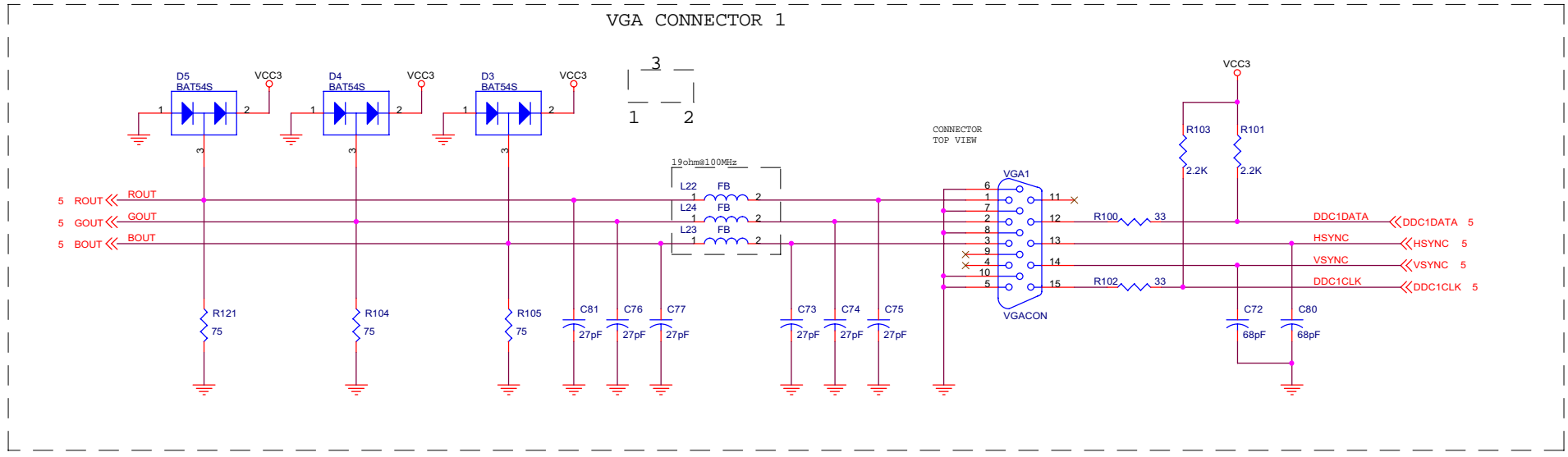
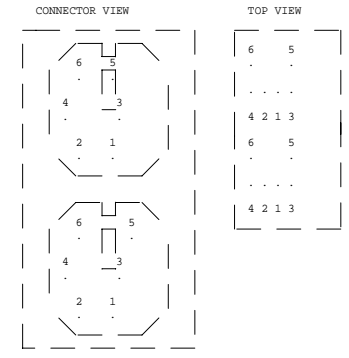
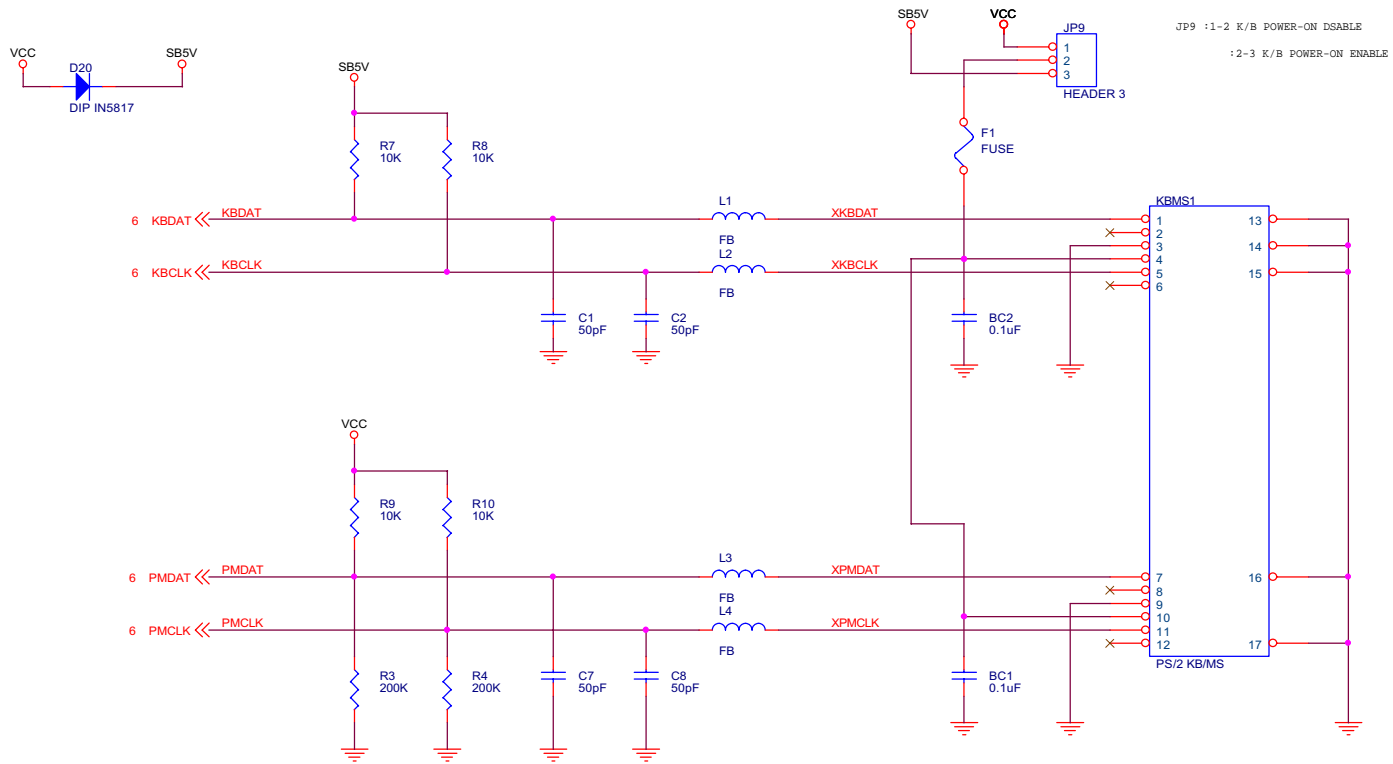


JET WAY INFORMATION		
Title PCI CONNECTOR 3&4		
Size B	Document Number J-630TCF	Rev 3.0
Date: Monday, October 22, 2001	Sheet 14	of 26



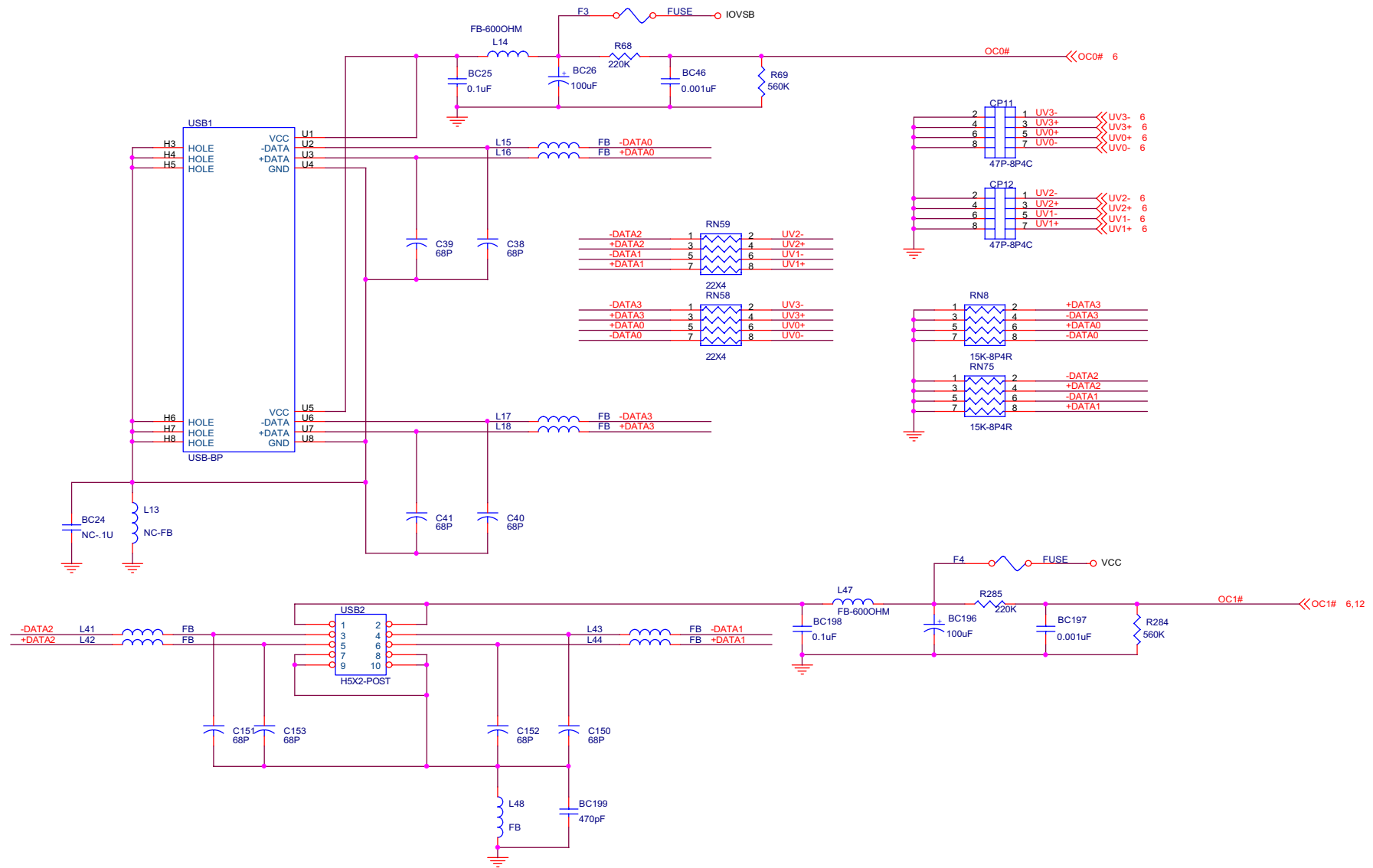
NOTE:
SIS IS NOT RESPONSIBLE FOR
ANY ERRORS OR OMISSIONS IN
THESE SCHEMATICS. THIS IS
AN EXAMPLE ONLY.

JET WAY INFORMATION		
Title IDE CONNECTORS		
Size B	Document Number J-630TCF	Rev 3.0
Date: Monday, October 22, 2001	Sheet 15	of 26

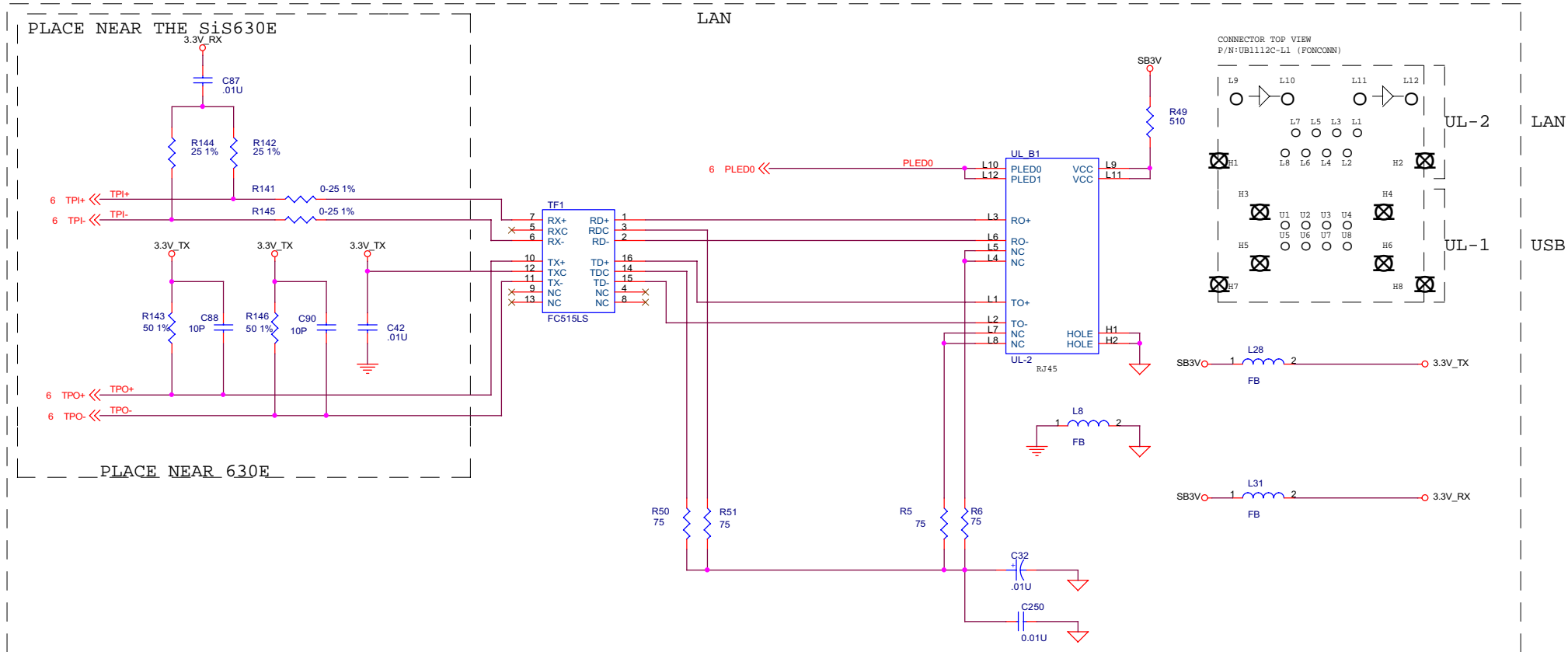


NOTE:
SIS IS NOT RESPONSIBLE FOR
ANY ERRORS OR OMISSIONS IN
THESE SCHEMATICS. THIS IS
AN EXAMPLE ONLY.

JET WAY INFORMATION		
Title KEYBOARD & MOUSE CONNECTORS		
Size B	Document Number J-630TCF	Rev 3.0
Date: Monday, October 22, 2001	Sheet 16	of 26

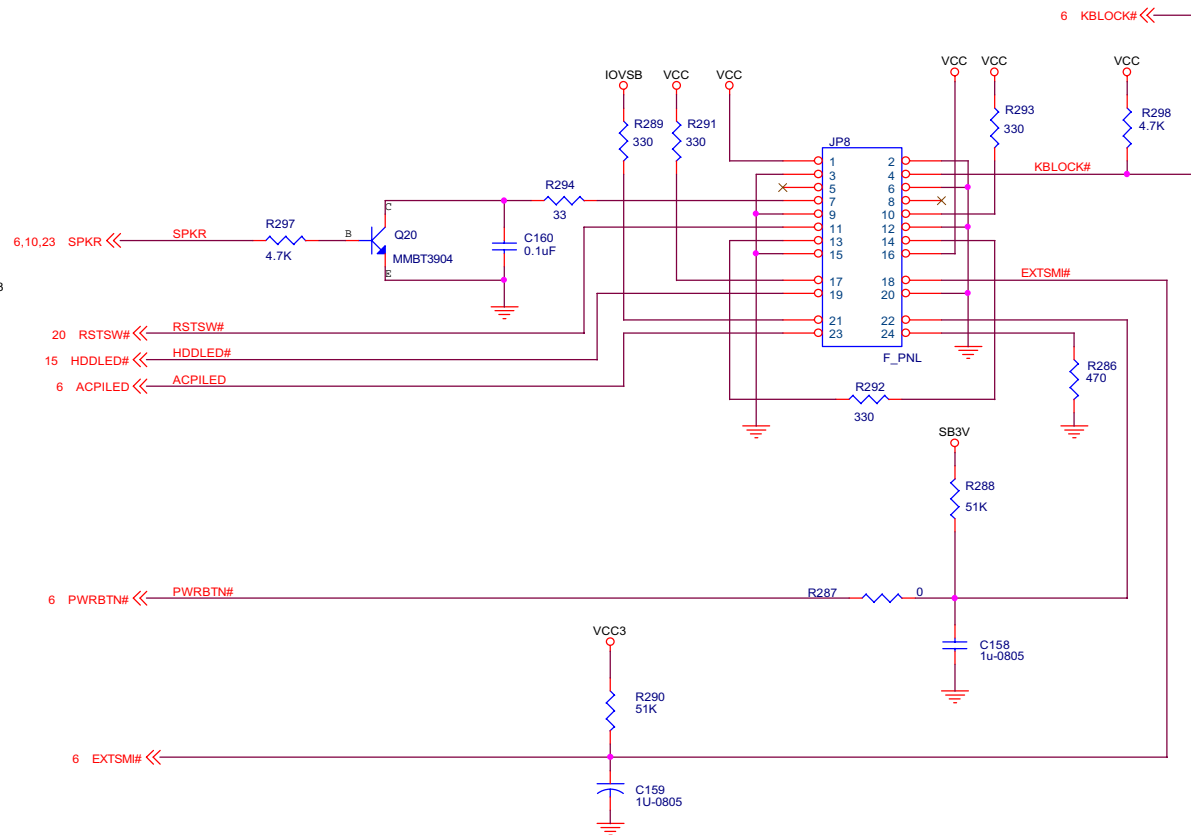
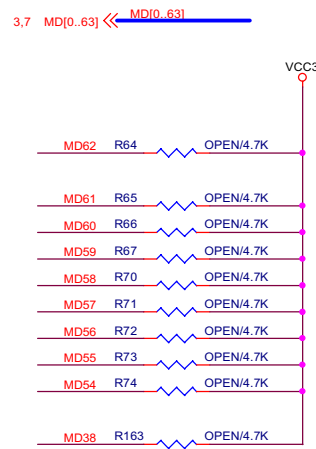


JET WAY INFORMATION		
Title USB CONNECTORS		
Size B	Document Number J-630TCF	Rev 3.0
Date: Monday, October 22, 2001	Sheet 17	of 26

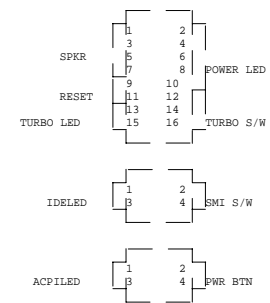


NOTE:
SIS IS NOT RESPONSIBLE FOR
ANY ERRORS OR OMISSIONS IN
THESE SCHEMATICS. THIS IS
AN EXAMPLE ONLY.

JET WAY INFORMATION			
Title		NETWORK OPTION 1	
Size	Document Number	Rev	
B	J-630TCF	3.0	
Date:	Monday, October 22, 2001	Sheet	18 of 26

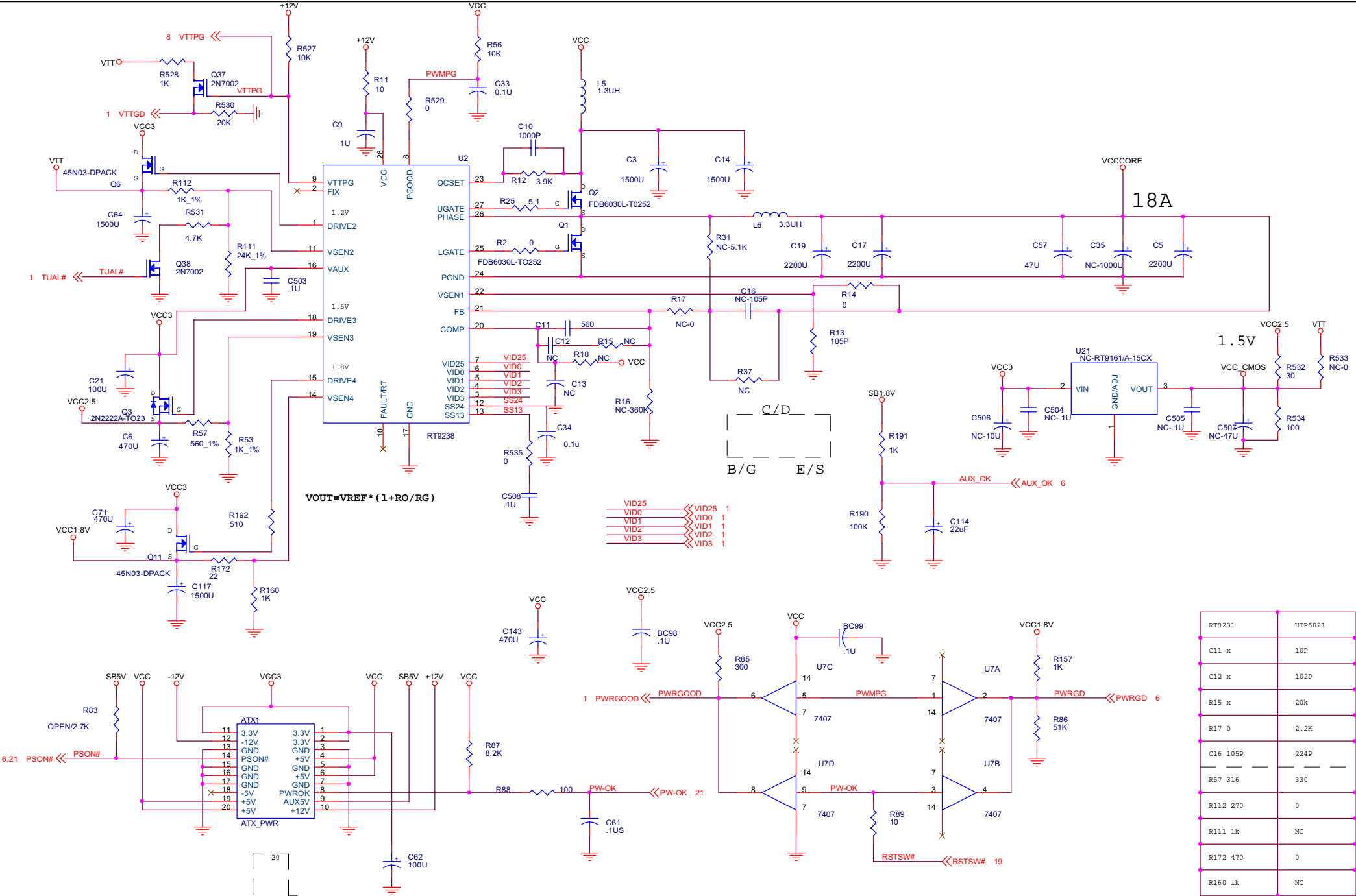


- MD62: PCI Clock PLL Enable
- MD61: SDRAM Clock DLL Enable
- MD60: CPU Clock DLL Enable
- MD[59..58]: SDRAM Clock DLL'S DRC[1..0] (Default 00)
- MD[57..56]: CPU Clock DLL'S DRC[1..0] (Default 00)
- MD[55..54]: PCI Clock DLL'S DRC[1..0] (Default 00)
- MD32: 0=NTSC / 1=PAL
- MD38: Enable INTERRUPT



NOTE:
SIS IS NOT RESPONSIBLE FOR ANY ERRORS OR OMISSIONS IN THESE SCHEMATICS. THIS IS AN EXAMPLE ONLY.

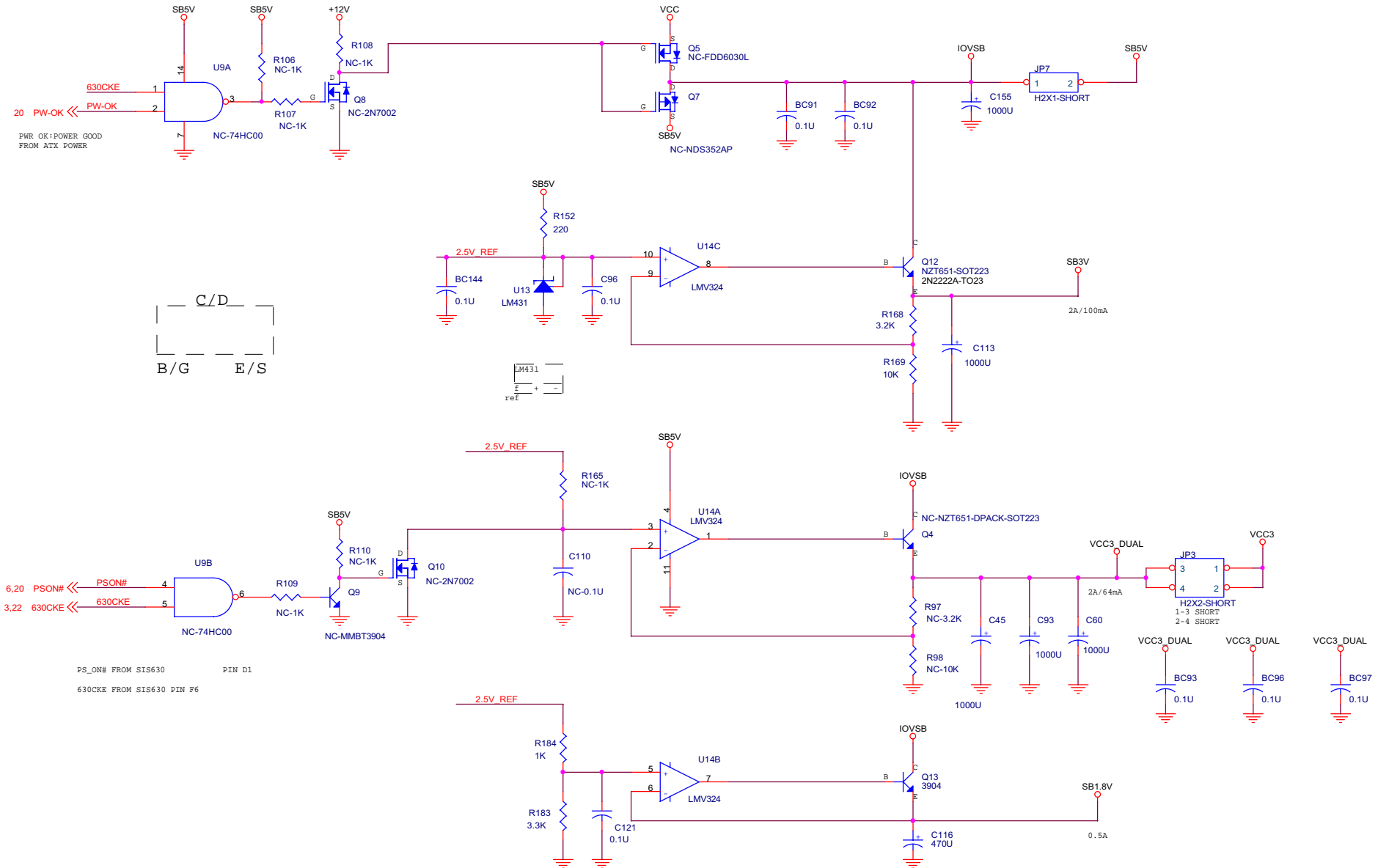
JET WAY INFORMATION		
Title DATA ACQUISITION & JUMPERS		
Size B	Document Number J-630TCF	Rev 3.0
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RT9231	HIP6021
C11 x	10P
C12 x	102P
R15 x	20k
R17 0	2.2K
C16 105P	224P
R57 316	330
R112 270	0
R111 1k	NC
R172 470	0
R160 1k	NC

JET WAY INFORMATION		
Title	HIP6021	
Size B	Document Number	Rev
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RC5058+Discrete ACPI FOR SIS630 - PAGE 2



JET WAY INFORMATION		
Title DISCRETE ACPI FOR SIS630 - 2		
Size B	Document Number J-630TCF	Rev 3.0
Date: Monday, October 22, 2001	Sheet 21 of 26	

W83697HF

(To monitor battery voltage, this input should be connected directly to battery)

Temperature Sensing

Voltage SENSING

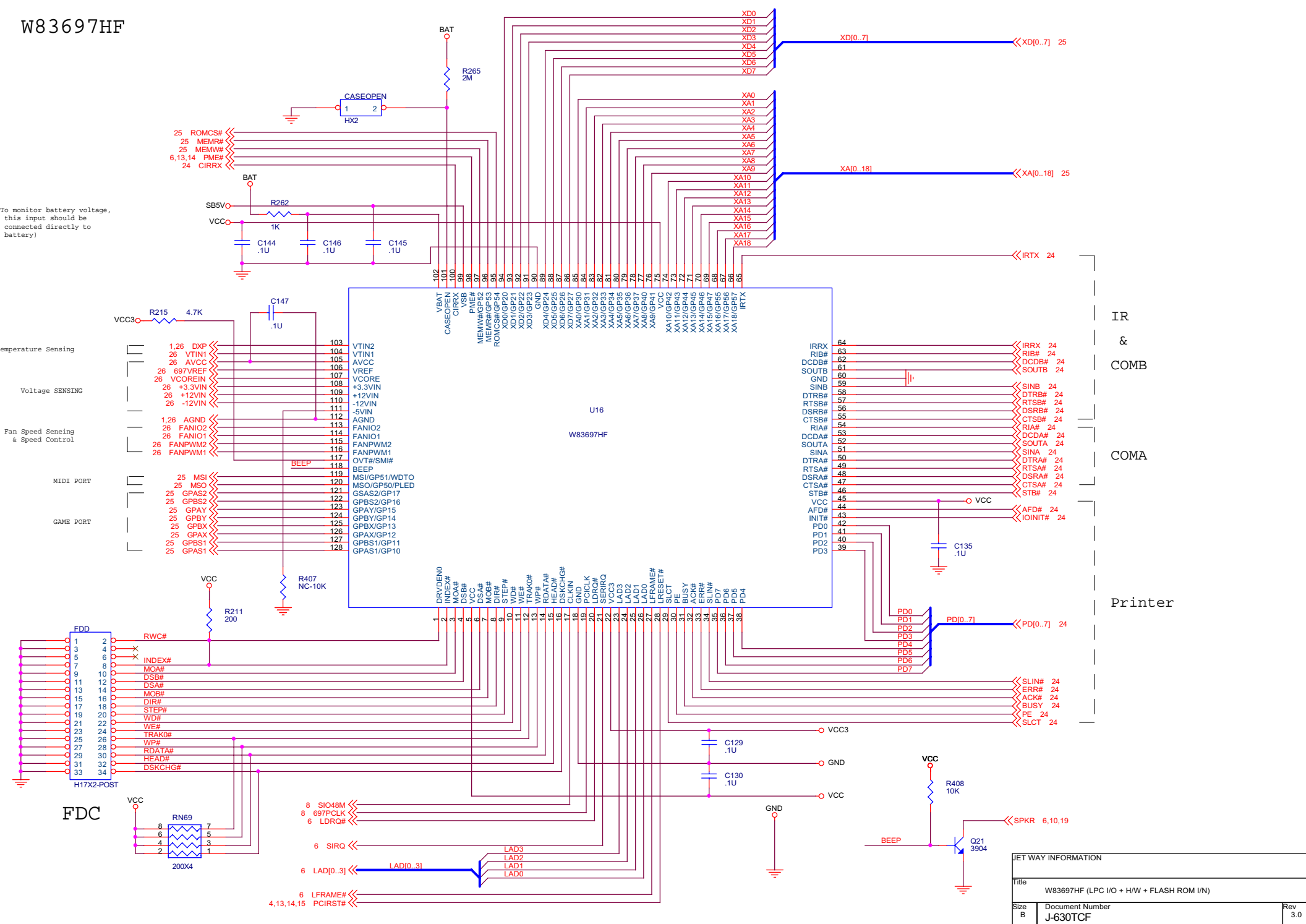
Fan Speed Seneing & Speed Control

MIDI PORT

GAME PORT

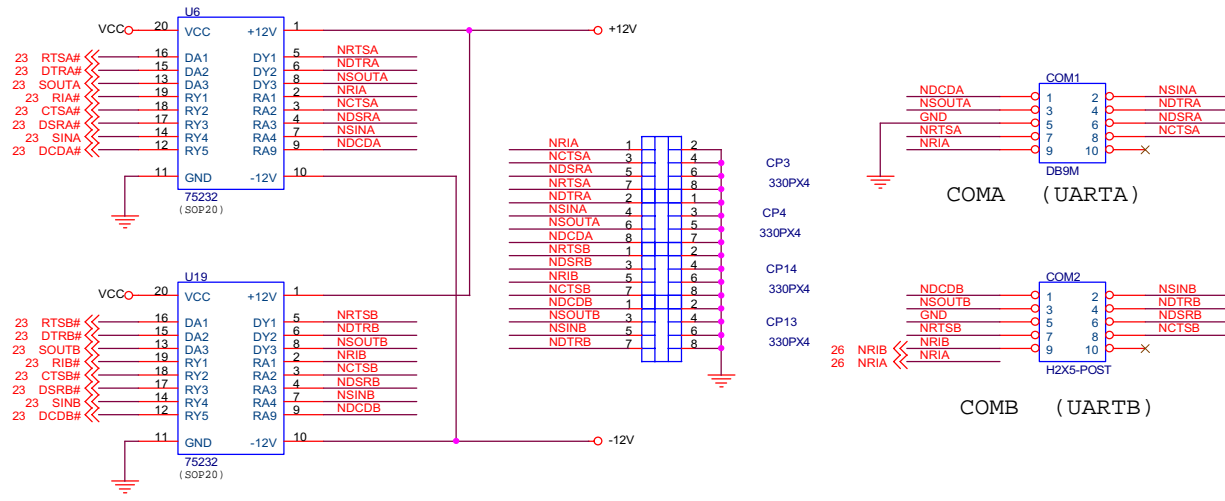
FDD

FDC

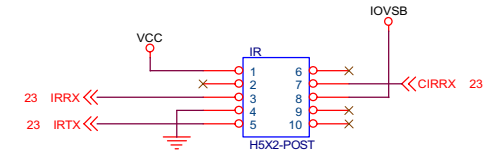


JET WAY INFORMATION		
Title	W83697HF (LPC I/O + H+W + FLASH ROM I/N)	
Size	Document Number	Rev
B	J-630TCF	3.0
Date:	Monday, October 22, 2001	Sheet 23 of 26

COM PORT

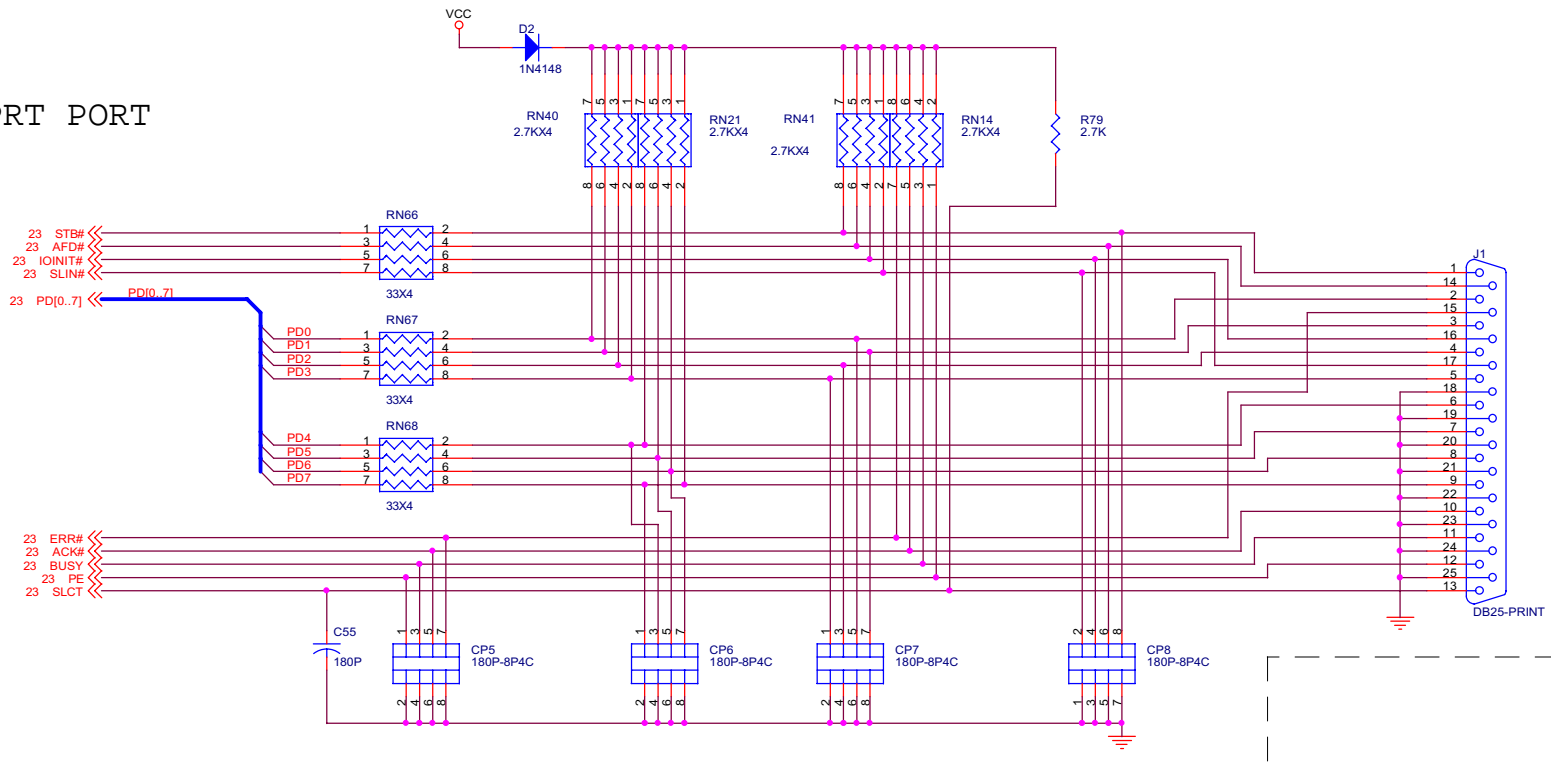


IR/CIR CONNECTOR



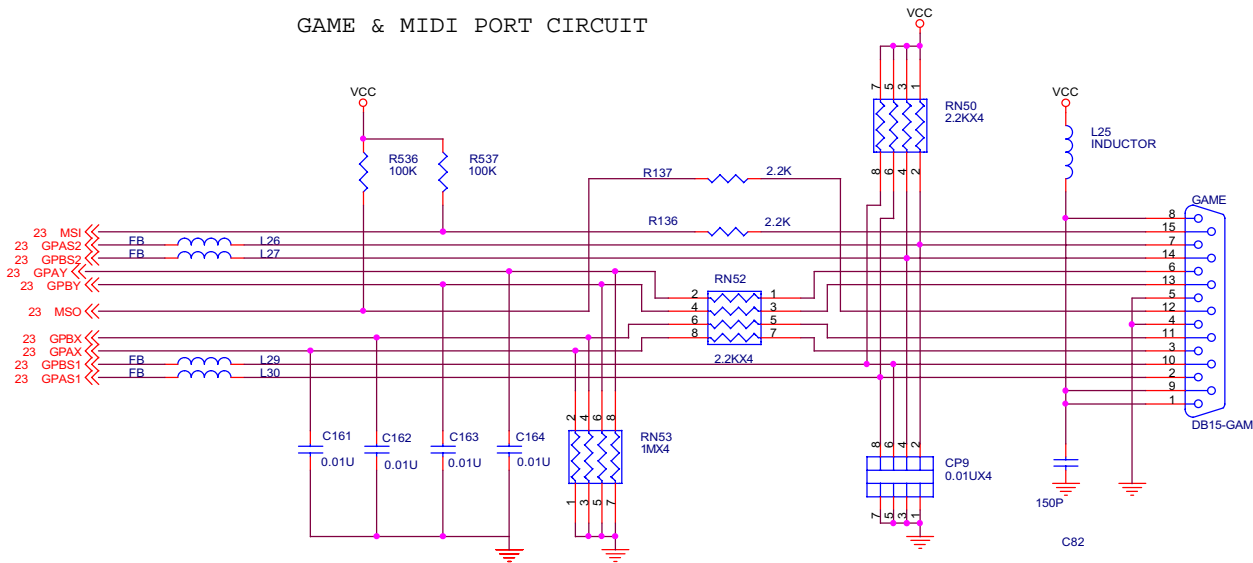
THE IOVSB OF PIN 3 IS FOR CIR WAKE-UP FUNCTION.

PRT PORT

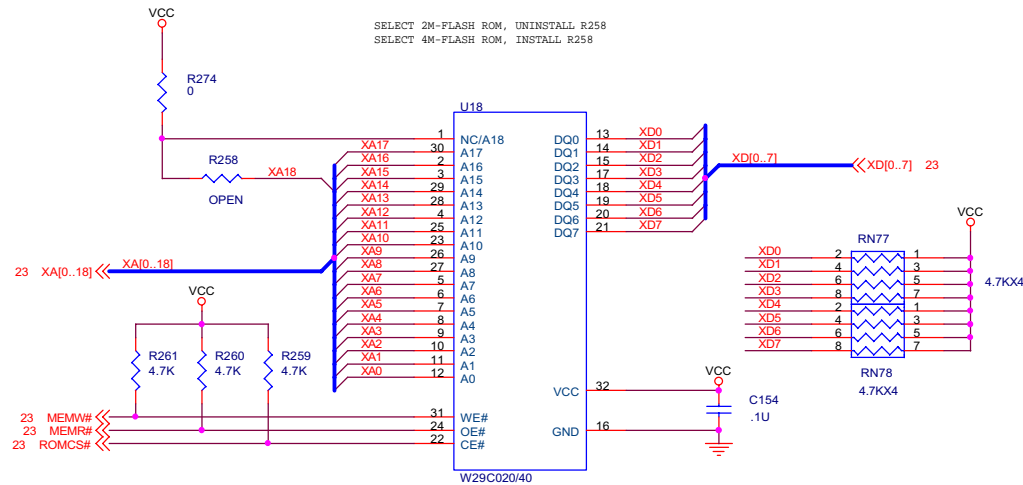


JET WAY INFORMATION		
Title	W83697HF (LPC I/O + H/W + FLASH ROM I/F)	
Size B	Document Number	Rev
	J-630TCF	3.0
Date:	Monday, October 22, 2001	Sheet 24 of 26

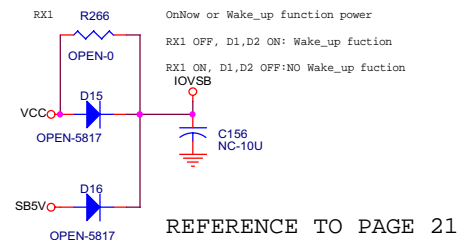
GAME & MIDI PORT CIRCUIT



FLASH ROM



IOVSB CIRCUIT



JET WAY INFORMATION

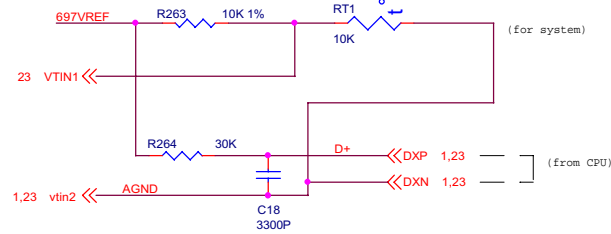
Title W83697HF (LPC I/O + H/W + FLASH ROM I/F)

Size B Document Number J-630TCF Rev 3.0

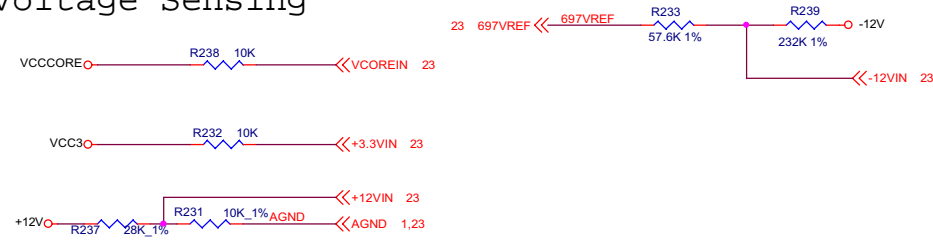
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Hardware Monitor circuits

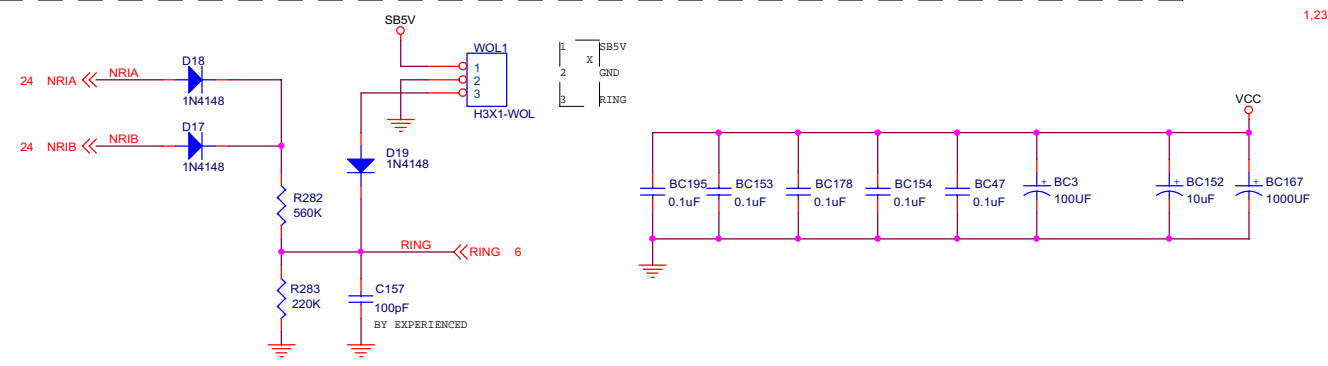
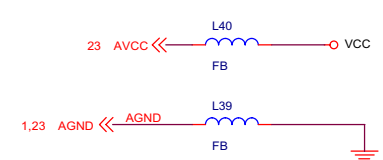
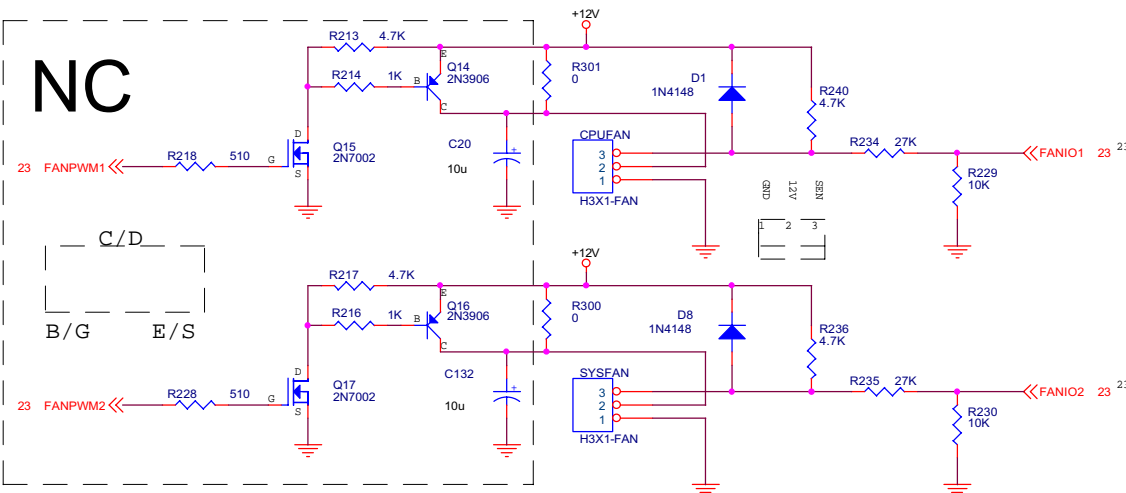
Temperature Sensing



Voltage Sensing



PWM Circuit for FAN speed control



JET WAY INFORMATION		
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